A 10μA On-chip Electrochemical Impedance Spectroscopy System for Wearables/Implantables

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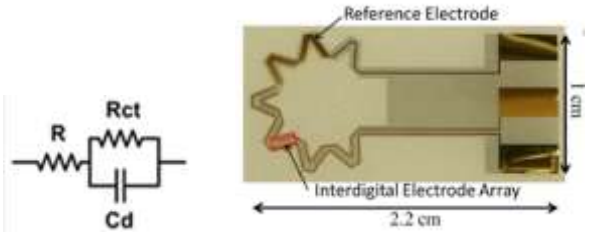
***Abstract*— This work proposes a new time-domain integration method to realize Electrochemical Impedance Spectroscopy (EIS). Unlike traditional EIS systems which use a quadrature sinusoid stimulus, we propose a low-frequency, low-amplitude sinusoid stimulus, which is realized through a sinusoid DAC without the need for analog filter. The error caused by harmonic generation can be suppressed through integration in detection. The response current is sensed by a switched capacitor integrator with control synchronized with sinusoid DAC. The integration output is sampled and digitized by an 8-bit SAR ADC. The (1×1.1)mm^2 prototype is fabricated in a 130nm CMOS process. It consumes 10μA from a 1.2V supply.**

Keywords— Electrochemical Impedance Spectroscopy, sinusoid DAC, time-domain integration

I. INTRODUCTION

There is an increasing demand for biofilm monitoring for wearables and implantables. Electrochemical Impedance Spectroscopy (EIS) is a popular method of quantitative and qualitative monitoring of biofilm. [1]. The electrical property of an EIS sensor interface can be modeled as a complex impedance shown in Fig.1 (a). When biofilm forms on a sensor, the complex impedance is modified [2]. A small amplitude and variable frequency sinusoid is applied between sensor electrodes. By comparing the amplitude and phase difference between the input signal and its response current, the impedance, thus biofilm formation information is acquired [3].

Traditionally, a Fast Fourier Transform (FFT) or Frequency Response Analyzer (FRA) is used to realize EIS detection [5][6]. The imaginary and real part of target conductance (impedance) can be acquired through quadrature mixing. However, both of the methods require clean quadrature sinusoid stimulus. The high frequency harmonics, after quadrature mixing with themselves, also appear at DC at the output, resulting in error without any attenuation. Note that EIS requires a low frequency (0.1Hz~10 kHz) and low amplitude (<30mV) stimulus. As a result, power and area-hungry filters need to be designed after sinusoid generator. Therefore, most existing works used external equipment [7] or off-chip components [5] to ensure clean stimulus. We propose a time-domain integration method, which increases the immunity of the system to harmonics. As an example experiment, a miniature EIS sensor for biofilm detection on contact lens has been fabricated and tested, shown in Fig. 1 (b) [4]. This paper demonstrates a complete, fully-integrated on-chip EIS system commensurate with the business.



(a) (b)

Fig. 1 (a) Simplified equivalent circuit for EIS; (b) EIS sensor.

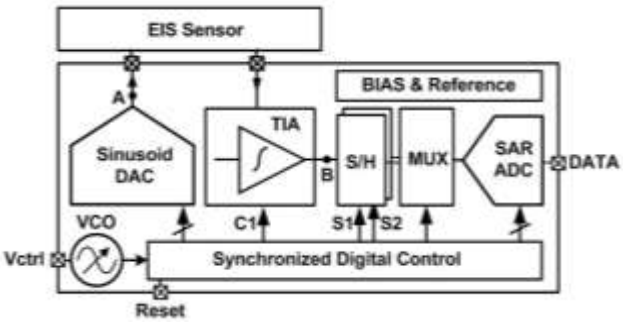


Fig. 2 Block diagram of the proposed EIS system.

II. PROPOSED DETECTION METHOD

To explain the function of integration on harmonic suppression, we first assume the stimulus applied to the impedance includes harmonics and therefore the response current also includes harmonics and can be formulated as:

$$I_{in} = Asin(\omega t) + Bsin(2\omega t) + Csin(3\omega t) + \cdots \quad (1)$$

If we integrate the current over a capacitor C_{int}, the output can be expressed as:

$$V_{out} = \int \frac{I_{in}dt}{C_{in}} \quad (2)$$

$$= -\frac{1}{\omega C_{in}}\left[Acos(\omega t) + \frac{B}{2}sin(2\omega t) + \frac{C}{3}sin(3\omega t) + \cdots\right]$$

From (2), the high frequency harmonic components are degraded with a ratio of 1/N (N is the frequency ratio of the high frequency component to the fundamental tone). The integrator has effectively suppressed the error caused by harmonics in stimulus. Based on this method, a time-domain integration EIS system is designed in Fig. 2. The stimulus is

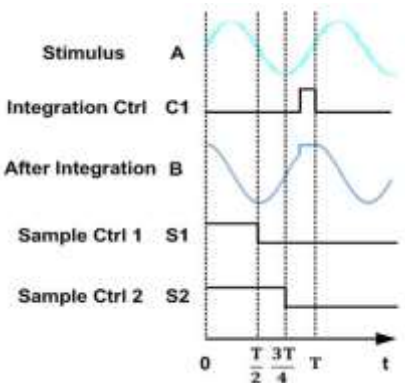


Fig. 3 Time domain signal showing system timing.

generated by a sinusoid DAC and the current response is integrated through a switched capacitor Integrator. The system is controlled through synchronized digital controls on chip. A ring oscillator VCO provides a fully-integrated clock for the system.

To explain the impedance characterization function of the proposed system, the time domain waveforms of key blocks are shown in Fig. 3. Assume the phase shift introduced by impedance is $\emptyset$, then the response sinusoid current can be expressed as:

$$I_{in} = I_A \sin(2\pi f t + \emptyset) \tag{3}$$

Where the amplitude is I_A. After integration on capacitor C_{int} in TIA, the output of the TIA at B is:

$$V_{\text{int}} = \frac{I_A}{2\pi f C_{int}} [\cos(2\pi f t + \emptyset) - \cos(\emptyset)] \tag{4}$$

If this voltage is sampled at T/2 and 3T/4, we arrive at:

$$V_{\frac{T}{2}} = -\frac{I_A}{2\pi f C_{int}} * 2\cos(\emptyset) \tag{5}$$

$$V_{\frac{T}{2}} = \frac{I_A}{2\pi f C_{int}} * [\sin(\emptyset) - \cos(\emptyset)] \tag{6}$$

Equation (5) (6) show that the two samples only include two variables: phase $\emptyset$ and amplitude I_A of the target conductance (impedance). The phase and amplitude information can be extracted with mathematical calculation shown as below:

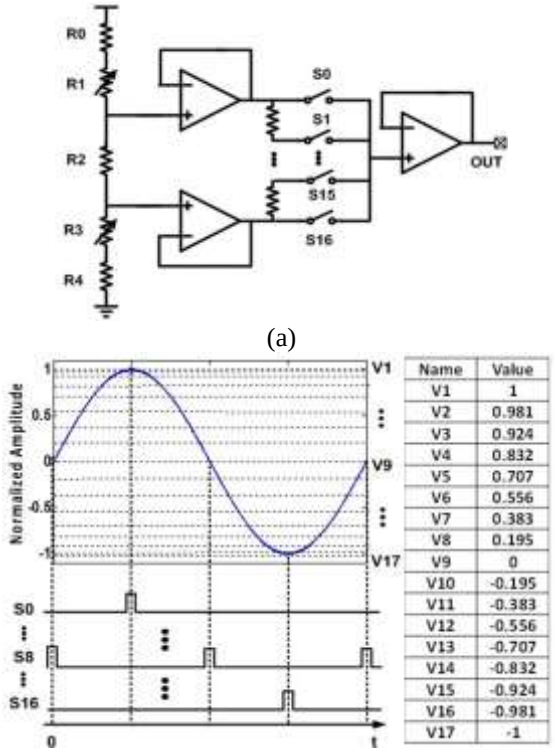
$$I_A = \frac{1}{2} * \sqrt{\left(V_{\frac{T}{2}}\right)^2 + \left(V_{\frac{T}{2}} - 2 * V_{\frac{3T}{4}}\right)^2} \tag{7}$$

$$\varphi = artan(\frac{V_{\frac{T}{2}} - 2 * V_{\frac{3T}{4}}}{2V_{\frac{T}{2}}}) \tag{8}$$

I. CIRCUIT IMPLEMENTATION

A. Sinusoid DAC

A sinusoid DAC is designed with segmented resistor references shown in Fig. 4 (a). The amplitude is defined by the first resistor string and the 17 voltage references are defined by the second resistor string. The 17 voltage references are chosen



Name	Value
V1	1
V2	0.981
V3	0.924
V4	0.832
V5	0.707
V6	0.556
V7	0.383
V8	0.195
V9	0
V10	-0.195
V11	-0.383
V12	-0.556
V13	-0.707
V14	-0.832
V15	-0.924
V16	-0.981
V17	-1

Fig. 4 The proposed sinusoid DAC: a) basic structure; b) digital control and reference selection.

by sampling the ideal sinusoid with a 32 over-sampling rate, as shown in Fig. 4(b). This work removes the low pass filter after the sinusoid DAC, resulting in high frequency harmonics at the output. As discussed in section II, the proposed time-domain integration detection method can attenuate the error caused by those harmonics. To ensure the reasonable system error, the ratio of clock frequency of the DAC over the generated frequency is carefully chosen. By comparing the TIA output with ideal sinusoid and sinusoid DAC, a ratio of 32 is chosen. This allows an amplitude and phase detection error below 5% in simulation.

B. Sinusoid Detection

The integrator-based trans-impedance amplifier (TIA) is shown in Fig. 5. In order to keep the response current proportional to the target transconductance (impedance), the common-gate transistor M0 with gain boosting is added to ensure low input impedance at the input node. The input impedance can be expressed as in (9). In this design, I0 is copied from the current mirror on chip to bias M0. Through feedback, the input node voltage is also set to Vcom, which is the same as the sinusoid generator DC output. The drain voltage of M0 is set by the bias voltage of integrator Vcom2. To ensure that M0 works in saturation, we make Vcom2 – Vcom = 200mV. Active current mirror loaded differential to single-end one stage opamp is used in the design. Note that opamp A and M0 contribute little noise to the input referred current noise. The main contribution of noise is current source I0, since the noise is added at output directly and the current gain is unity.

$$Z_{in} = \frac{1}{A * gm_{m0}} \tag{9}$$

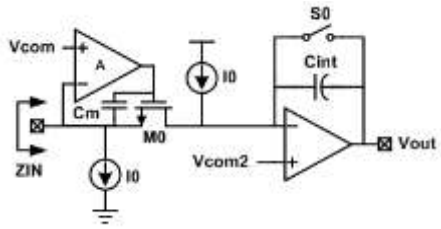


Fig. 5 The proposed EIS detection circuit.

In this design, the gm of key MOSFETs has been increased to push the noise frequency corner to low frequency. Large device areas were chosen to decrease 1/f noise. Note that integration capacitor in this work is fixed, but can be extended into a capacitor array in the future to expand dynamic range. The proposed TIA is followed by a sample and hold. The sampled results are converted into a digital value through a low power 8 bit SAR ADC.

C. Synchronized Digital Control

According to the timing requirements shown in Fig. 3, the DAC, integration control, sample and hold, and ADC are all synchronized through digital control on chip. To decrease system power, the sample and holds are conducted every 8 integration cycles. The ADC clock is therefore slowed down to provide 2 samples every 4 integration cycles. Moreover, considering that the speed of the system is slow, data can be collected and averaged to reduce error.

II. MEASUREMENT RESULTS

The proposed system was fabricated in a 130nm CMOS process. The die photo is shown in Fig. 6. The whole system consumes 10uA under a 1.2V supply. The synchronized digital control signal for the system and the output data are tested through an oscilloscope and the result is shown in Fig. 7. Note that DATA_EN is the signal used to flag the start of series data.

The sinusoid generated on chip can sweep from 900Hz to 2.8 kHz. The performance of the sinusoid DAC is shown in Fig. 8 and Fig. 9. As related in Section III, the filter has been omitted in this system, resulting in replicas, about -30dB lower than the fundamental tone in the output. The error caused by these replicas can be eliminated by time-domain integration.

In order to validate the function of the proposed time-domain detection method, an ideal sinusoid is fed in through a

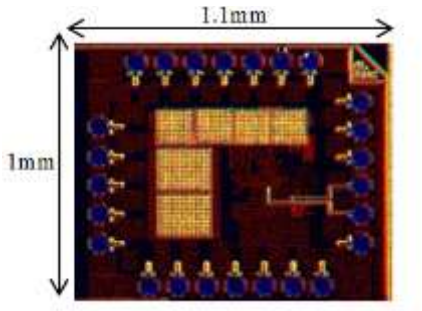


Fig. 6: Die photo of the EIS chip

signal generator and synchronized by the on-chip integration control signal. System function is tested by comparing an ideal input with a recovered phase and amplitude from the test result. Fig. 10 shows the two test results: by a) fixing phase and sweeping the input sinusoid amplitude; b) fixing amplitude and sweeping the input sinusoid phase. The test error of the amplitude and phase are all below 3%.

System function with both the sinusoid generator and the sinusoid detector is tested with a sensor model. The test data,

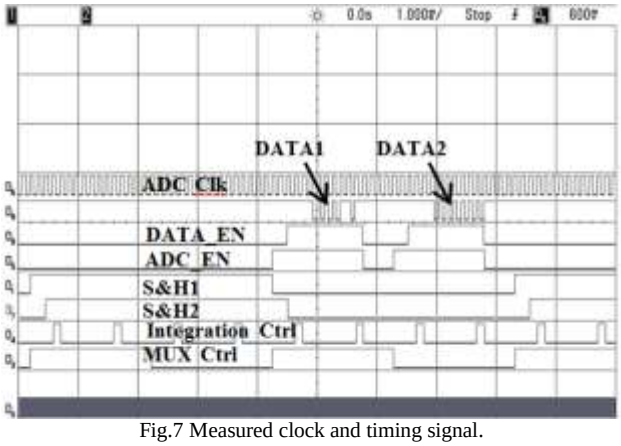


Fig.7 Measured clock and timing signal.

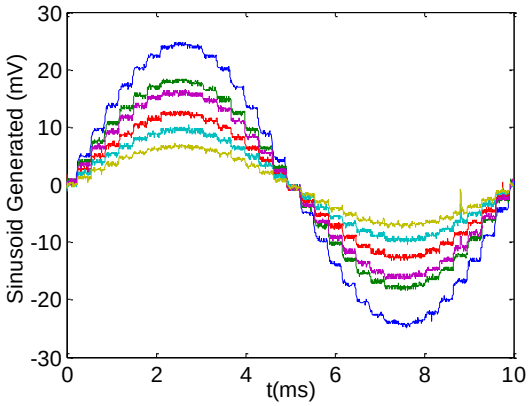


Fig. 8: Sinusoid DAC output cross amplitude setting.

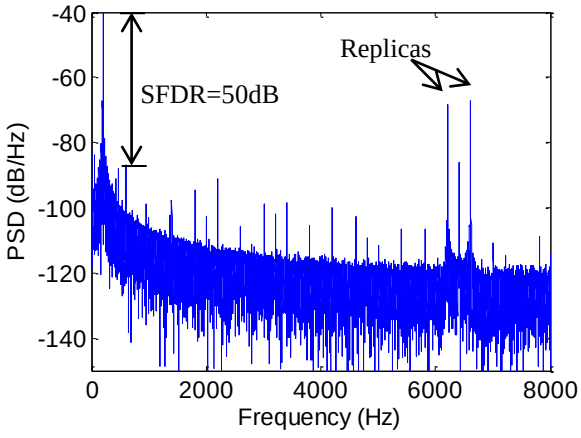


Fig.9: FFT of generated 1KHz sinusoid.

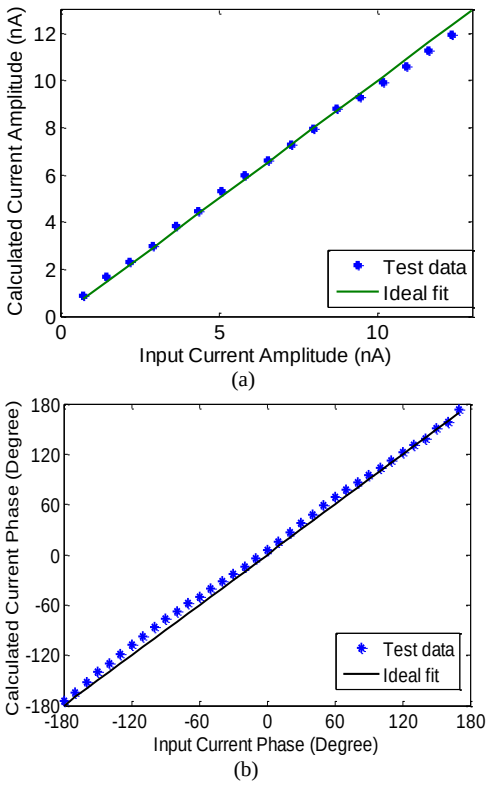


Fig. 10: Proposed detection function test with ideal sinusoid current with a) Fixed phase and sweep amplitude; b) Fixed amplitude and sweep phase.

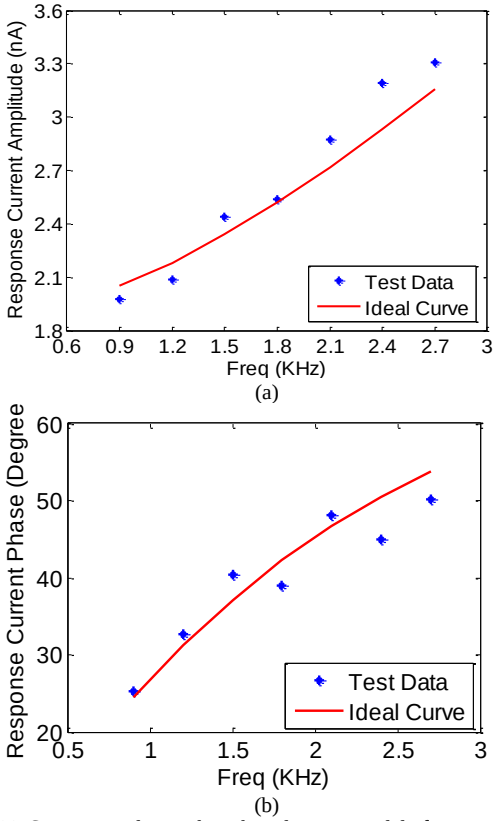


Fig. 11: System test data with on-board circuit model of sensor: (a) target conductance (impedance) amplitude change according to frequency sweep; (b) target conductance phase change according to frequency sweep.

shown in Fig. 11, is collected with R=100 Ω, Cd=20pF and Rd=4 MΩ in Fig. 1(a). The amplitude error is below 5% and the phase error is below 8%. The results demonstrate the error caused by sinusoid generator nonlinearities have been mitigated through the proposed method. Table I provides an analysis of the presented design: compared to existing impedance spectroscopy systems, this work achieves the lowest power and lowest area with a reasonable error.

TABLE I. PERFORMANCE COMPARISON OF IMPEDANCE SENSING INTERFACE

System	This work	ISSCC 10 [5]	JSSCC 09 [7]	TBCAS 12 [6]
Technology	0.13µm	0.35µm	0.5µm	0.13µm
Power/Channel	12µW	0.85mW	0.3mW	42uW
Area	0.6mm^2	4mm^2	2.25mm^2	1.68mm^2
Supply	1.2V	3.3V	3V	1.2V
Resolution	8b	16b	8b	9.3b
Stimulus Generator	Yes	No	No	Yes
Off-chip Auxiliary	No	Yes	Yes	Yes
Error	8%	N.A.	0.3%	8%

III. CONCLUSION

A time-domain integration EIS system is presented. Compared with traditional structure, the proposed system does not require clean quadrature sinusoid stimulus and therefore do not need power and area hungry analog filters. As a result, a low-power low-complexity EIS system is realized with a reasonable error. The impedance spectroscopy microsystem was implemented in a CMOS 130nm technology. The whole system consumes 10µA from a 1.2 V supply.

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