A -173 dBc/Hz @ 1 MHz offset Colpitts Oscillator using AlN Contour-Mode MEMS Resonator

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Abstract - **A differential Colpitts oscillator using AlN MEMS CMR designed in 0.13 um CMOS is presented in this work. The oscillator operates at 1.16 GHz, with a total power consumption of 4.2 mW at 1 V supply. It achieves a phase noise of -143.6 dBc/Hz, -173.3 dBc/Hz at 100 kHz and 1 MHz offset frequency respectively with a figure of merit (FOM) of 228.3 dB. Current-based temperature compensation was employed to reduce oscillator drift across temperature.**

I. INTRODUCTION

Low power and low noise RF frequency generators are essential for applications such as high performance ADCs, high speed serial data links, and low power radios [1]. Micromachined Aluminum Nitride (AlN) Contour-Mode-Resonators (CMRs) show an enormous opportunity in high performance RF frequency generation. These resonators have a Q-factor over 100 times that of on-chip inductors. Their integration on wafer or package can effectively replace large off-chip crystals and SAWs.

Due to their small-form factor, high frequency of operation, and capability to be co-integrated with CMOS circuits, MEMS resonators are a candidate for the implementation of compact and multi-frequency banks of high-quality-factor mechanical elements that can be used for the synthesis of next-generation reconfigurable local oscillators for radio frequency (RF) transceivers [2-3]. In this work, we focus on AlN Contour-Mode Resonators (CMRs). The high transduction efficiency of the piezoelectric film translates to low values of achievable motional resistance (tens of ohms).

Modern telecommunication systems require oscillators that are stable over a wide range of parameters, including vibration and temperature [4]. In high precision commercial oscillators, either temperature compensated crystals (TCXO) [5] or oven stabilized devices (OCXO) [6] are used. Other work demonstrates an embedded ovenization technique to decrease temperature dependence of the resonance frequency down to less than a few ppm (< 2ppm) [12]. However, most of the existing ovenization techniques are aimed for compensating the temperature dependence of the resonator only. To achieve less than 1 ppm frequency variation, any contributions from CMOS and passive devices in the circuit should be taken into account as well.
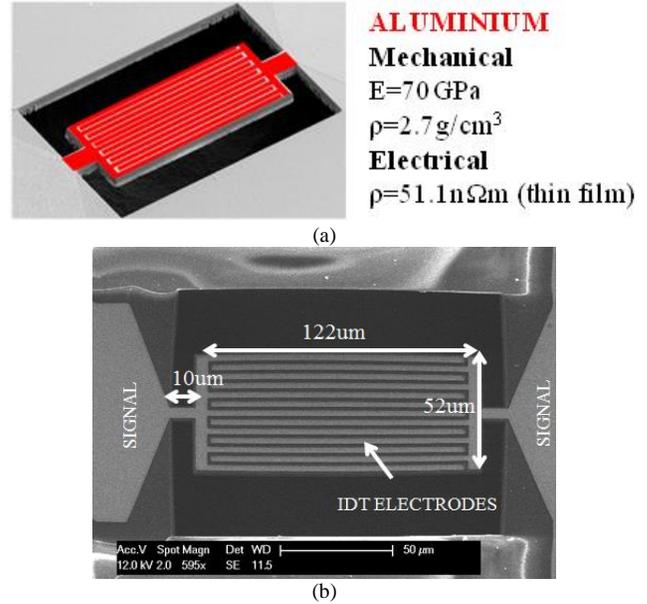

(a)

(b)

Fig. 1 1GHz Resonator : (a) AlN contour mode resonator with aluminium top metal electrodes and (b) SEM pictures of it.

There are two key contributions of this work. First, we demonstrate an extremely low oscillator phase noise floor resulting from a co-design of the MEMS resonator with a CMOS oscillator. Secondly, we introduce a bias technique to reduce the oscillator temperature coefficient when using an ovenized resonator. The resonator and sustaining oscillator are presented in section II. Section III explains in more detail how the current source compensates the frequency drift caused by the components in the oscillator. The test result follows in section IV.

II. DIFFERENTIAL COLPITTS OSCILLATOR & AIN MEMS CMR

The resonator in this work is formed by a 4 µm thick piezoelectric plate. It is covered by the IDT electrodes layer, which is made of 100nm Al thin film deposited straight on the silicon substrate. The dimensions of the resonator plate are 52×122 um^2. For the fabrication, high resistivity Si wafer is
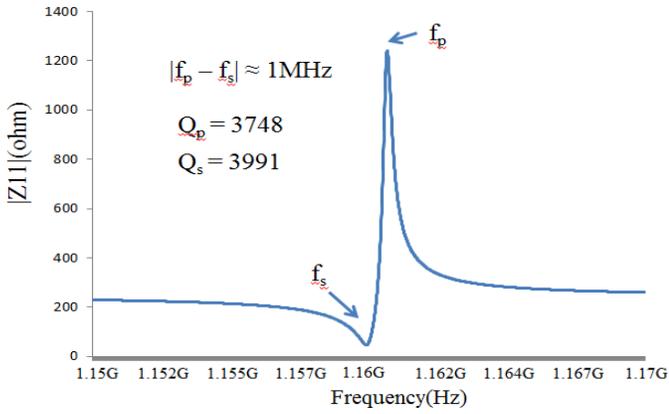
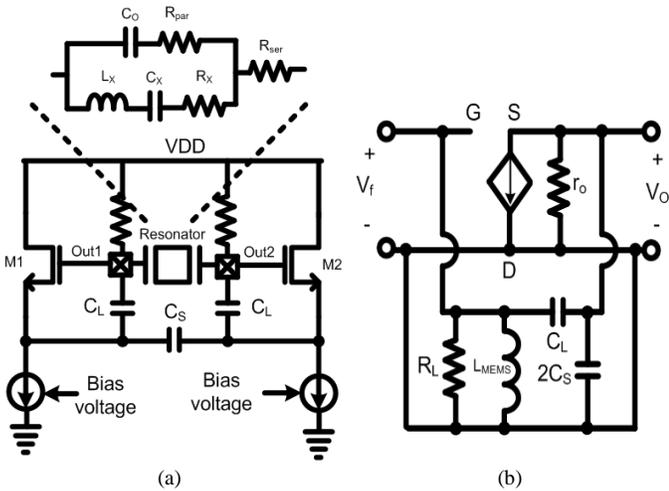Fig. 2 Impedance magnitude of the resonator when loaded by oscillator capacitance.

Fig.4 Single ended model of the differential Colpitts oscillator

$$w_{osc} \cong \sqrt{\frac{gmL_{MEMS} + R_L(C_s + C_L)}{L_{MEMS}C_sR_LC_L}} \quad (gmr_o \gg 1) \quad gmR_B > \frac{C_L}{2C_S} \quad (1)$$

In order to decrease the phase noise of the oscillator, the noise contribution of each active device needs to be carefully analyzed. The differential oscillator is converted to a single ended, as shown in Fig.4, thus leading to equation (2) [8].

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{4kT\delta g_{m1}}{g_{m2}^2} + \frac{4kT\delta g_{m3}}{g_{m2}^2} + \frac{4kT\delta}{g_{m2}} \quad (2)$$

Based on this equation, the transconductance of M2 needs to be increased to minimize the noise.

III. CURRENT SOURCE FOR TEMPERATURE COMPENSATION

The dominant source of the resonance frequency drift over temperature variation is the resonator (-22ppm/C). In the field of crystal oscillators, temperature compensated crystal oscillators (TCXO) [5] and oven stabilized devices (OCXO) [6] are often employed. In contrast, this work is targeted at a microscale heater contained in the resonator itself. This heater reduces the temperature drift from the resonator to 2ppm [12]. However, to achieve less than one ppm frequency variation, the CMOS circuit related contribution must be considered as well since the heater does not stabilize the temperature of the oscillator. Fig.6 shows the frequency variation, when the temperature coefficient of current source is zero and ideal resonator (no temperature dependent) are used, which reveals the inherent frequency drift due to temperature resulting from the CMOS circuitry.

To reduce the drift due to CMOS, we must design a current source that compensates for the temperature drift of the oscillator. The addition-based current source is a good candidate to stabilize oscillator frequency variation due to the CMOS temperature coefficient [10]. Though its aim is for compensating bias current variation caused by process variation, we can modify the structure to allow temperature compensation. The proposed technique allows us to tune the temperature coefficient of the current reference to cancel residual frequency drift.

Fig.3 (a) Differential Colpitts Oscillator and (b) its small signal model

employed. Fig.1(a) depicts the electrode of the resonator and its properties. An SEM of the entire structure is shown in Fig.1(b).

Fig. 2 shows the magnitude of impedance of the resonator when loaded with the oscillator capacitance. In this figure k_t^2 is proportional to the difference between the parallel (f_p) and series (f_s) resonance frequency and has a value of 0.99%. The quality factor (Q) of the unloaded parallel resonance is around 3,700.

In an unloaded condition, when R_p is 48 kΩ, in parallel resonance mode, the Colpitts oscillator senses the voltage from the tank of the resonator. Due to the series and parallel parasitic capacitance, the frequency difference between f_s and f_p is decreased from 5 MHz to 1 MHz in the case of loaded condition. The effects to the phase noise performance due to the decrease in k_t^2 will be explained further in section IV.

To utilize this AlN CMR, the differential Colpitts oscillator was designed as shown in Fig.3. The equivalent small signal model allows calculation of the conditions for oscillation, leading to the equation (1). To sustain oscillation, C_S is chosen to have a large value and hence the capacitance ratio between C_L and C_S becomes smaller than $g_m \cdot R_B$.
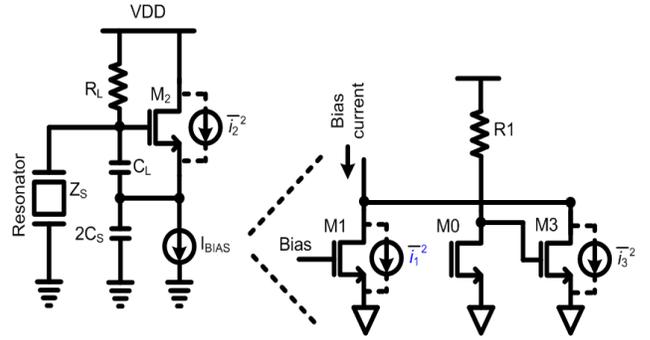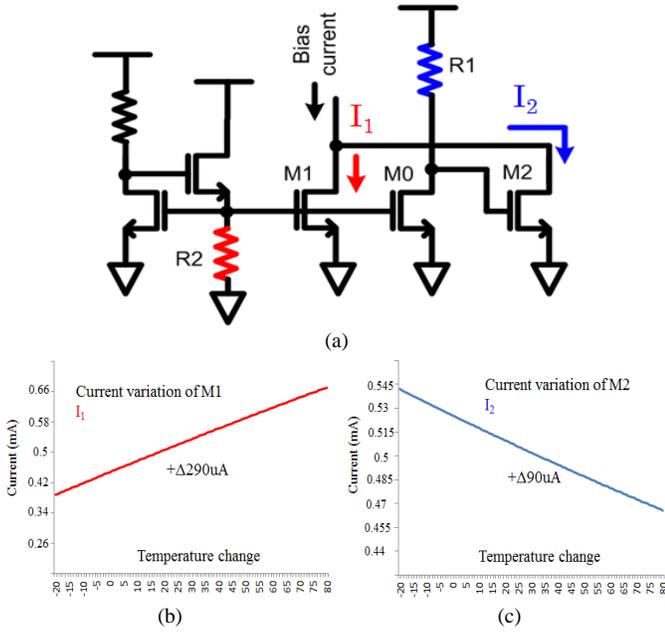
(a)

(b)   (c)

Fig.5 (a) Proposed current source and the current variation of M1(b), M2(c) under the temperature change (Simulation).
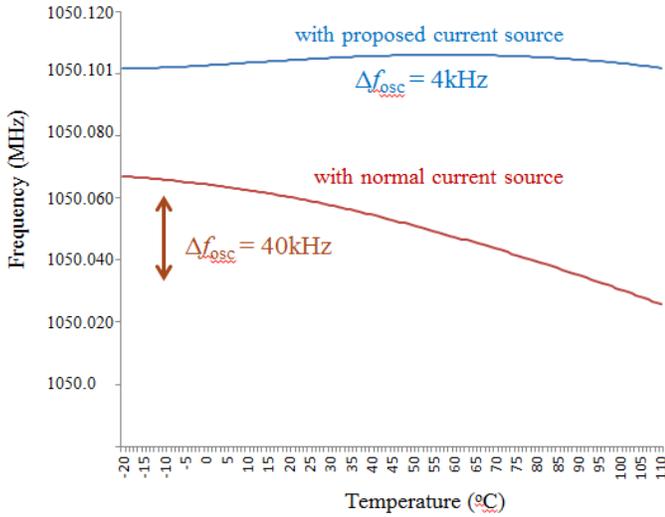

Fig.6 Simulation result of resonance frequency variation with and without proposed current source.

(a)

(b)

Fig. 7 (a) Test bench for the proposed current source and (b) test result

Fig.5(a) is a block diagram of the proposed current source to compensate the frequency variation caused by oscillator. The two poly bias resistors (R1 and R2) are identical in value and layout. The resistance variation dominates the temperature coefficient of the current reference. The resistors have a positive temperature coefficient, leading to a decrease in current in M2 as temperature increases. Conversely, the current through M1 increases, allowing cancellation and tuning of the current temperature coefficient. Fig.5(b) and (c) shows these behaviors. The simulated frequency drift of the oscillator, assuming the resonator temperature is completely stabilized and current source has zero temperature coefficient is 40 kHz (simu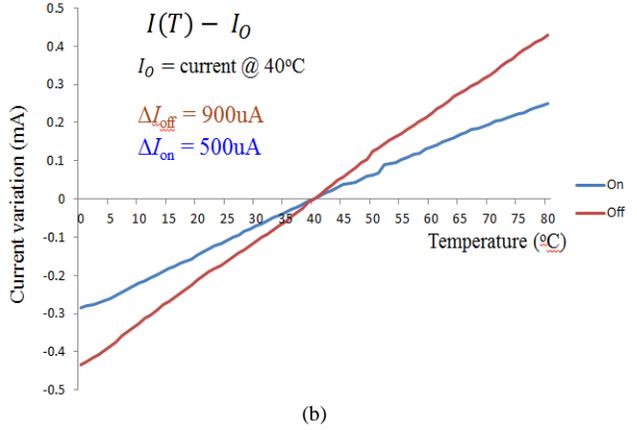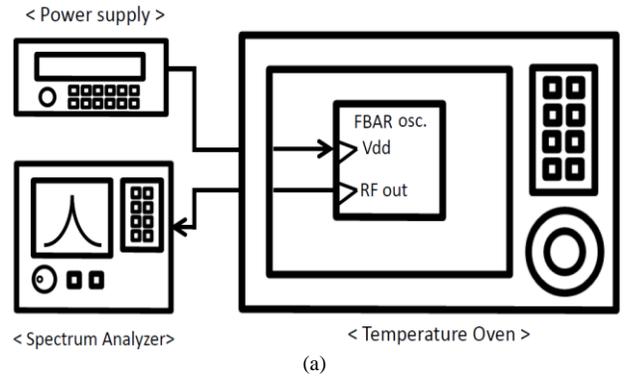lated). With this proposed current source having total bias current with a positive temperature coefficient, the oscillation frequency variation is decreased to less than 4 kHz (simulated). To verify this effectiveness, the test bench is set up as shown in Fig.7(a). As the temperature is swept from 0 ^{o}C to 80 ^{o}C, the total frequency change is -1777 ppm which is equal to -22ppm/^{o}C when the temperature compensating function is off. But, when the modified current source is on, the total frequency variation is decreased by 25 kHz over the whole temperature range, which means the frequency variation caused by oscillator decreases. Of course, the temperature variation due to the resonator remains. However, as mentioned above, using an ovenized resonator should allow us to get expected temperature coefficients around 1 ppm.. Fig.7(b) shows the test result of a current variation with and without this current source, demonstrating the ability to tune the current temperature coefficient.

IV. TEST RESULT

To test the phase noise of this high Q (low noise) oscillator, the noise floor inherent in the test equipment should be considered. Fig. 8 is the measured phase noise result. The dots in the plot represent the noise floor of the test equipment (Agilent Technology E5052B). At around 1 MHz offset frequency, there is a dip in the phase noise response. This feature is consistent with the difference in f_s and f_p (roughly 1 MHz). We believe this dip in phase noise is due to a reduction in tank impedance at f_s. Fig. 2(b) shows that the
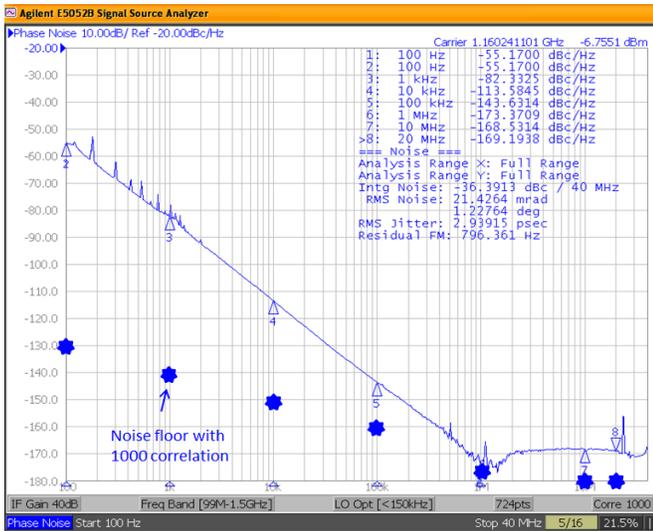
Fig.8 Phase noise measurement with 1000 correlations.

	f_{osc} (GHz)	Power (mW)	Tech.	Phase noise @10kHz (dBc/Hz)	Phase noise @100kHz (dBc/Hz)	Phase noise @1MHz (dBc/Hz)	FOM
This work	1.16	4.2	0.13um CMOS, MEMS	-113.5	-143.6	-173.3	**228.3**
[11]	1.55	11.3	0.13um CMOS, FBAR	-	-	-144.3	197
[12]	0.585	10	GaAs P-HEMT	-120	-145	-155	200.3
[13]	2	0.025	0.18um CMOS, FBAR	-	-121	-140	222
[14]	0.6	5.6	0.13um CMOS, FBAR	-126	-140	-150	198
[15]	1.5	1	0.35um CMOS, FBAR	-112	-133	-147	210

Table 1 Performance comparison with the previous work.

impedance of the resonator is at a local minimum at f_s. Table 1 shows the performance comparison with the previous works based on the phase noise at 1 MHz offset frequency and power consumption. The FOM is described in equation below. $L(\Delta f)$ represents the absolute value of the phase noise, and f_o, Δf are center frequency and offset frequency respectively.

$$\text{FOM} = L(\Delta f) + 20\log\left(\frac{f_o}{\Delta f}\right) - 10\log P(mW)$$

Fig. 9 shows the die photo of the realization. The AlN MEMS CMR on the left side is wirebonded directly to the differential Colpitts oscillator.

V. CONCLUSION

This work exploits the high Q of AlN MEMS CMRs to achieve good phase noise performance. The phase noise at 1 MHz offset frequency is -173.3 dBc/Hz. The measured jitter (integrated from 12 kHz to 40 MHz) is 2.9 ps rms. The center frequency of this oscillator is 1.16 GHz, and it is fabricated
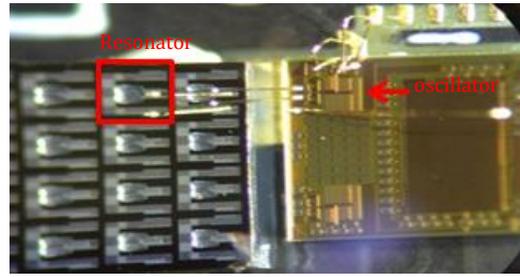

Fig.9 Die photo of the oscillator and resonator.

using 130nm CMOS technology. The next step will be employing an ovenized resonatorin order to decrease the temperature stability of the overall circuit in the entire temperature rangeto sub-ppm levels.

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