

A 20 mV Input Boost Converter With Efficient Digital Control for Thermoelectric Energy Harvesting

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Abstract—This paper presents a low power boost converter for thermoelectric energy harvesting that demonstrates an efficiency that is 15% higher than the state-of-the-art for voltage conversion ratios above 20. This is achieved by utilizing a technique allowing synchronous rectification in the discontinuous conduction mode. A low-power method for input voltage monitoring is presented. The low input voltage requirements allow operation from a thermoelectric generator powered by body heat. The converter, fabricated in a 0.13 μm CMOS process, operates from input voltages ranging from 20 mV to 250 mV while supplying a regulated 1 V output. The converter consumes 1.6 (1.1) μW of quiescent power, delivers up to 25 (175) μW of output power, and is 46 (75)% efficient for a 20 mV and 100 mV input, respectively.

Index Terms—Boost converter, discontinuous conduction mode, energy harvesting, low power, low voltage, power scavenging, pulse-frequency modulation, synchronous DC-DC converter.

I. INTRODUCTION

FOR wireless systems such as implantable medical sensors and animal tracking devices, battery replacement may be difficult or impossible. Emerging battery-free power sources (small thermoelectric generators, individual solar cells, microbial fuel cells) provide significantly less than the voltage required (around 1 V) for most state-of-the-art integrated circuits. For example, thermoelectric energy harvested from machines, aircraft, and even body heat can be used as a virtually indefinite power supply for such circuits. However, there are many challenges associated with converting thermal energy from body heat to electrical energy [1], [2]. A thermoelectric generator (TEG) generates a voltage that is proportional to the difference of the temperatures applied to each side. One side is placed either on the warm skin or under the skin, while the other side is exposed to the cooler ambient air. Although the body temperature of the subject is well regulated, the ambient temperature, airflow, and thermal insulation due to clothing varies widely. Therefore, a DC-DC converter that can accommodate a widely-varying and low voltage source and boost it to a regulated supply is needed to operate low-power circuitry. Because our target load circuitry consumes 10 μW of average power or less, the

converter must have very low quiescent power consumption in order to efficiently drive the low-power load. This paper presents a switched-mode boost converter that can step up voltages between 20 mV and 250 mV to efficiently provide a controllable voltage of approximately 1 V to a 10 μW load. Section II explains the control method used to achieve synchronous rectification in discontinuous conduction mode (DCM) that facilitates efficient low-voltage low-power operation. Section III provides an overall block diagram of the boost converter circuit with descriptions of each block. Section IV explains how design parameters were optimized to maximize efficiency. Section V presents measured results and compares to the state-of-the-art.

II. SYNCHRONOUS RECTIFICATION THROUGH PEAK CURRENT-MODULATION

A diagram of an ideal boost converter is shown in Fig. 1(a). Boost converters typically operate in one of two modes: continuous conduction or discontinuous conduction [3]. The main difference is that, in the continuous conduction mode (CCM), the inductor current can flow negative if the load is small enough. In contrast, in the discontinuous conduction mode (DCM), the inductor current is prevented from flowing negative. The DCM is more efficient when the average input current is less than half the ripple current because the CCM will discharge the output capacitor during the part of the switching cycle when the inductor current flows negative, increasing switching losses [4]. By utilizing pulse-frequency modulation (PFM), the efficiency can be further improved at low power levels because the switching losses scale with the output power. As illustrated in Fig. 2, when operating in the DCM, the high-side switch turns off before the current flows negative, thereby maximizing the net charge placed on the output capacitor per switching cycle. Using a diode for the high-side switch, as shown in Fig. 1(b), would be inefficient due to the high forward voltage drop. A pFET can be used as the high-side switch to avoid this voltage drop, as in Fig. 1(c). The challenge therefore is in synchronizing the high-side switch with the moment that the current falls to zero (T_{fall}).

A. Synchronous Rectification Methodologies

For maximum efficiency, the pFET should turn off just as the inductor current falls to zero. A feedback mechanism is needed to drive the current zero-crossing as close as possible to the pFET turn-off instant (T_P). One technique is to use a reactive gate control method that uses a comparator to detect when the pFET becomes reverse biased and subsequently trigger a pulse to disable the switch [5]. This method is problematic because it requires a very fast (on the order of 1/4 the pFET on-time of 40 ns) comparator evaluation and gate driver for the pFET. Significant latency in the detection process will allow the inductor

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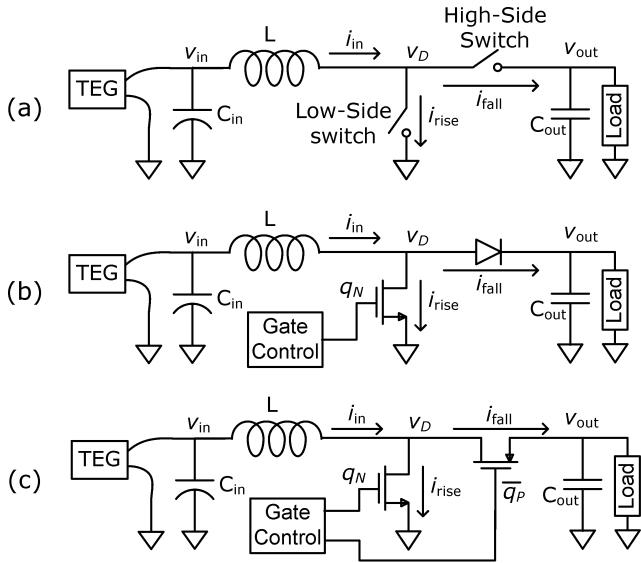


Fig. 1. A boost converter using (a) ideal switches, (b) a diode as the high-side switch, and (c) a pFET as the high-side switch, to step up voltage from a TEG to drive a low-power load.

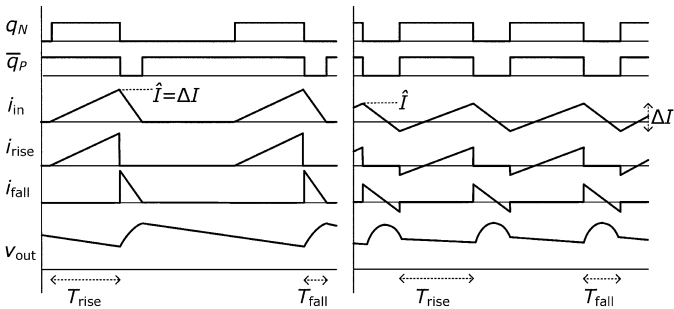


Fig. 2. Discontinuous conduction mode (left) is more efficient than continuous conduction mode (right) at low power levels because it does not allow the current through the pFET high side switch to flow negative.

current to flow negative, dramatically reducing the converter efficiency. An offset can be introduced into the comparator to counteract the latency, as described in [6], but this method is subject to variations in the slope of the falling current waveform i_{fall} . An alternative is to use an adaptive circuit that senses when the pFET turns off, compares that to when the pFET becomes reverse biased, and adjusts the time duration that the pFET is on for the next cycle accordingly [7]. Though this solution solves the latency problem, it still requires a comparator to sense the polarity of the current. Since the target quiescent power dissipation is around $1 \mu\text{W}$, static comparator bias current is undesirable.

B. Proposed Method

Our proposed synchronization method, illustrated in Fig. 3, requires no analog circuitry and is thus nearly free of static current dissipation. If the pFET is turned off early (before the inductor current falls to zero), the pFET will continue to conduct, but with a much higher voltage drop. The result is that the V_D node stays high, even after the pFET is switched off. The voltage will stay high until the inductor current finally falls to zero. On

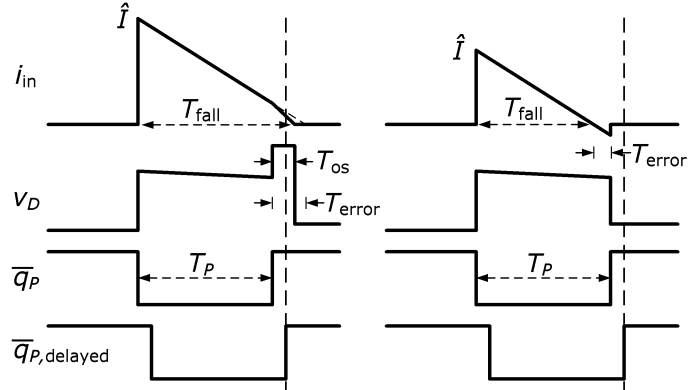


Fig. 3. Left: If the power FET drain voltage (v_D) is high after the pFET is switched off, then the current fell to zero after the pFET was switched off. Right: If the drain voltage is low after the pFET is switched off, then the current fell to zero before the pFET was switched off.

the other hand, if the pFET is turned off late, the V_D voltage will fall to zero very quickly after the pFET is finally switched off. Since only the logic level of V_D needs to be detected, a static CMOS flip-flop can be used for the operation. Therefore, by sampling the high/low state of the drain voltage shortly after the pFET is switched off, one can determine whether the pFET was turned off before or after the current falls to zero.

The logic threshold of the flip-flop is skewed high (more than 50% of the output voltage) in order to quickly detect when v_D transitions low and also to prevent a false reading from ringing on the V_D node. The duration of the delay is set as short as possible while ensuring that across process/voltage/temperature (PVT) the delay is always longer than the time it takes the V_D node to transition low (assuming zero inductor current at the time that the pFET is switched off). If the delay is too fast, the flip-flop will always sample the V_D node to be high. The width of the v_D overshoot pulse T_{os} is proportional to the delay time. It is desirable to minimize the width of this overshoot pulse because during that time the pFET is conducting with a much higher resistance.

To synchronize the pFET turn-off with the inductor current zero-crossing, we have chosen to adjust the peak current \hat{I} instead of the pFET switch timing T_P . Increasing \hat{I} , for example, increases the time that it takes the current to fall to zero (T_{fall}). This choice is appropriate since the nFET on-time is much longer than the pFET on-time, and thus easier to control. The peak current is adjusted by changing the duration that the nFET switch is on (T_{rise}). The current rise-time (T_{rise}) is set by the frequency of the on-chip oscillator that drives the nFET gate. The frequency control circuit in Fig. 4 adjusts the oscillator frequency to make T_{fall} equal to T_P . The flip-flop samples the binary state of the V_D voltage shortly after the rising edge of the pFET gate voltage. The sampled state informs the counter to either count up (decrease the oscillator period) or count down (increase the oscillator period). Thus, the counter acts as an integrator in the feedback loop. If the sampled state is high, then the counter increments and T_{rise} , \hat{I} , and T_{fall} all decrease for the next switching cycle. If the V_D state is low, then the counter decrements, causing T_{rise} , \hat{I} , and T_{fall} to increase for the next cycle. The result is that, in steady state, the current will

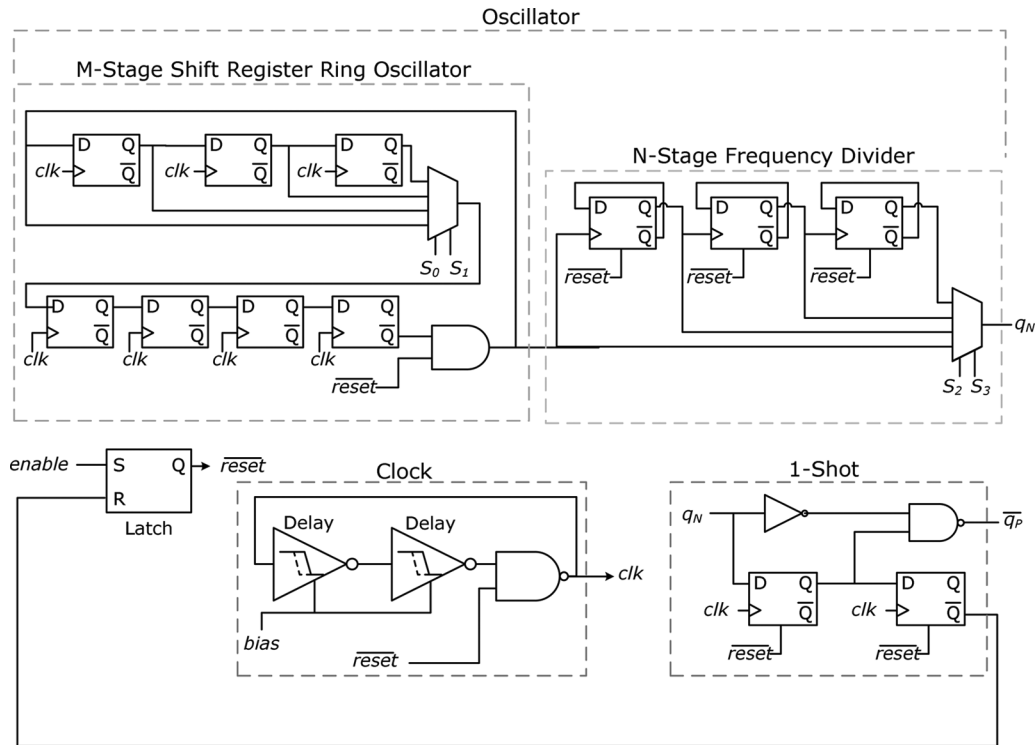


Fig. 6. Digitally controlled oscillator and one-shot block diagram.

Also, the circuit requires three off-chip passive components: and inductor and two filter capacitors.

A. Power FETs

The power FETs are dual-gate MOSFETs that can withstand drain-source voltages up to 2.6 V. The high voltage tolerance comes at the expense of higher channel resistance, but is needed because the drain voltage can exceed V_{out} plus V_{th} (which could total > 1.5 V). To avoid latch-up, the pFET and nFET were laid out with 30 μm spacing and surrounded by 10 μm guard rings.

B. Voltage Supervisor and Voltage Divider

The voltage supervisor and the bias circuitry are the only blocks that consume static power. This supervisor monitors the output voltage and activates an on-chip clock when the output voltage is below $2V_{\text{ref}}$. All circuits are idle until the voltage supervisor output transitions high. The voltage supervisor delay specifications are not stringent, though it is preferable to be faster than half the oscillator period (320 ns minimum period) to minimize output voltage ripple. A switched-capacitor voltage divider is used to scale down the output voltage before entering the voltage supervisor. The switched capacitor topology eliminates the static bias current inevitable with a resistive divider. Equal value switched capacitors provide an accurate 2X voltage division. Each capacitor is 0.9 pF, which is large enough such that the input capacitance of the voltage supervisor and other parasitic capacitances do not significantly affect the divided voltage (less than 5% error).

C. Oscillator and One-Shot

The oscillator and one-shot circuits set the on-time of the switching nFET (T_{rise}) and pFET (T_P), respectively. T_{rise} is equal to the duration that the oscillator is high for each cycle. T_P is equal to the clock period (40 ns) and is approximately equal to T_{fall} due to the synchronization feedback. From (1), it can be seen that in order to support an input voltage of 20 mV with an output voltage of 1 V, T_{rise} will be approximately 50 times greater than T_{fall} (in reality it will be about 60 due to voltage drop from parasitic resistances). For a 200 mV input, T_{rise} will be 4.5 times greater than T_{fall} . Therefore, the oscillator must have a controllable output pulse-width ranging between 4 and 60 times greater than T_P .

The oscillator circuit and the one-shot circuit are shown in detail in Fig. 6. A gated ring oscillator generates the 50 MHz clock that drives the control logic. The clock is enabled when the signal from the comparator transitions high. A latch prevents circuit interruption partway through a switching cycle. An external bias (supplied by I_{ref} in Fig. 4) allows external manipulation of the frequency for experimentation. Though we expect the frequency to have a significant temperature coefficient, the boost converter maintains functionality for frequency variations up to 25%. Because the oscillator and the one-shot circuits are driven by the same clock, this topology ensures that the time that the nFET is on (T_{rise}) is always a well defined multiple of the time that the pFET is on, T_P .

The oscillator circuit contains two sub-blocks. The shift register ring oscillator block creates a 50% duty cycle square-wave with a period adjustable by 40 ns steps. This signal then enters an N-stage frequency divider to allow a wide frequency control range. The result is a 50% duty cycle square wave that can have

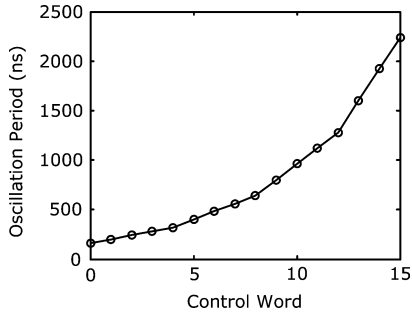


Fig. 7. Relationship between the oscillator output period and the digital input control word.

a period ranging from 320 ns up to 4480 ns (frequency range of 220 kHz to 3.1 MHz) with approximately 20% increments. This allows T_{rise} to be adjustable between 160 ns and 2240 ns while only requiring 4 control bits. The relationship between the input control word and the output period is shown in Fig. 7.

Reducing the quantization error of the controllable period by adding more control bits comes at the expense of circuit complexity and integrator (counter) response time. Since T_{rise} is only adjusted by one increment per switching cycle, a smaller step size would result in slower response times to sudden changes in input voltage. A 20% worst-case T_{fall} inaccuracy results from our 4-bit control, creating an approximately 5% reduction in efficiency. A 4-bit control word means that the worst-case time that it would take the oscillator frequency to increment to the steady-state value would be 15 switching cycles (20 μs for a 10 μW load).

The one-shot output feeds into the pFET gate driver. The one-shot circuit transitions low immediately after the nFET turns off (when the oscillator goes low) and stays low for one clock cycle (40 ns) before transitioning back high. Therefore, the duration that the pFET is on (T_P) is equal to the clock period. The peak inductor current \hat{I} is directly proportional to T_{fall} and T_P when the synchronization feedback is working properly. Therefore, the peak inductor current can be controlled by adjusting the clock frequency.

D. Zero Compare

To prevent the boost converter from pulling the TEG voltage below 20 mV, a switch (M_3 in Fig. 4) is used in the load current return path. When the digital control signal to the oscillator block reaches zero, the input voltage is considered critically low and the zero-compare circuit switches off the load in order to allow the input voltage to recover. Because the input voltage is so low, the internal control circuitry must be powered from the output of the converter. This means that the output capacitor must be charged to at least 600 mV before the boost converter can operate. If the stored output voltage drops below approximately 600 mV, the power FETs will fail to turn on sufficiently, creating a prohibitively large on-resistance and causing the circuit to fail.

E. Startup

A significant problem with this type of voltage converter is startup. For the conditions described in this paper, a one-time

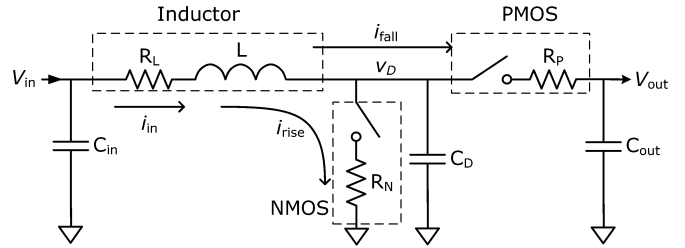


Fig. 8. Boost converter diagram showing the parasitic resistances of the power FETs and the inductor, along with the parasitic capacitance at the V_D node.

precharge of the load capacitor was used to startup the converter. If an energy storage element such as battery or supercapacitor is present in the system, it can store charge while the converter is disabled for long periods of time. When the voltage from the TEG returns to usable levels, the charge from the storage element would revive the converter. If the storage element is completely discharged, a low-power switched capacitor circuit could be used to generate the 600 mV needed for startup. Since a limited amount of energy is required for startup, the switched capacitor circuit needs neither high efficiency nor high output power.

F. Bias Generator and References

The bias generator distributes the necessary currents for the clock circuit and the voltage supervisor. This block consumes 200 nA (I_{ref}) from an externally generated current reference. An external voltage reference sets the regulated output voltage. A bandgap reference and regulator combination similar to the one in [9] can be used to generate on-chip references, which will consume approximately 250 nA of additional current, thereby reducing the overall efficiency by roughly 2% for a 10 μW load.

IV. DESIGN METHODOLOGY

Maximizing conversion efficiency is important when the input power comes from an energy harvesting device such as a TEG due to the inherent output power limitations of the TEG. In order to maximize the efficiency of the converter, one must understand the tradeoffs associated with each design choice. Design parameters such as the power FET sizes, peak inductor current, and inductor choice all need to be optimized to provide the best efficiency. However, functionality requirements such as limits on maximum output power, voltage ripple, and total die/PCB area must also be considered. Our design target was on for an input voltage of 50 mV, an output voltage of 1 V, and an output power of 10 μW .

A. Efficiency Calculation

A model was built to understand how each design parameter affects efficiency. Fig. 8 shows a representation of the boost converter including the primary sources of power losses. The inductor and power FETs each have parasitic resistances that result in conduction losses, and the parasitic capacitance at the V_D node along with the power FET gate capacitances cause switching losses. If we assume that the input voltage ripple and output voltage ripple are small, and the voltage drop from the parasitic resistances of the inductor and nFET are much smaller

than the input voltage, a reasonably accurate efficiency model can be derived [10].

The efficiency of the boost converter is

$$\eta = \frac{E_{\text{load}}}{E_{\text{in}}} \quad (2)$$

where E_{load} is the energy delivered to the load and E_{in} is the energy drawn from the source during one switching cycle.

Equation (2) can be expanded to show each source of losses:

$$\eta = \frac{E_{\text{out}} - E_{N\text{-drive}} - E_{P\text{-drive}} - E_D - E_{\text{ctl}} - E_{\text{sync}}}{E_{\text{out}} + E_{RN} + E_{RP} + E_{RL}} \cdot \frac{P_{\text{load}}}{P_{\text{static}} + P_{\text{load}}} \quad (3)$$

$E_{N\text{-drive}}$ and $E_{P\text{-drive}}$ are the energy required to drive the gates of the power nFET and pFET, E_D is the energy lost due to driving the parasitic capacitance on the V_D node, and E_{ctl} is the energy consumed by the control logic. E_{RN} , E_{RP} , and E_{RL} are the conduction losses due to the parasitic resistances of the nFET, pFET, and inductor, respectively. The final term takes into account the static power losses due to the voltage supervisor circuit.

E_{out} , the amount of energy that is converted to the higher voltage (V_{out}) per cycle, is

$$E_{\text{out}} = \frac{L\hat{I}^2}{2} + \frac{V_{\text{in}}\hat{I}T_{\text{fall}}}{2} - \frac{C_D V_{\text{out}}^2}{2} - \frac{\hat{I}^2(R_p + R_L)T_{\text{fall}}}{3} \quad (4)$$

where the first term is the energy stored in the inductor during T_{rise} , the second is the energy that enters the converter during T_{fall} , the third is the energy required to charge the C_D capacitance, and the final term is the energy lost due to the inductor and pFET parasitic resistances.

The rising time and falling time of the inductor current are

$$T_{\text{rise}} = \frac{L\hat{I}}{V_{\text{in}} - \frac{1}{2}\hat{I}(R_N + R_L)} \quad (5)$$

and

$$T_{\text{fall}} = \frac{L\hat{I}}{V_{\text{out}} - V_{\text{in}} + \frac{1}{2}\hat{I}(R_p + R_L)} \quad (6)$$

E_{sync} represents energy losses due to synchronization error of the power FET gate timing. If the pFET is turned off before the current reaches zero, the synchronization losses come from increased voltage drop of the pFET during the overshoot time (T_{os} , Fig. 3):

$$E_{\text{sync}} \approx \frac{\hat{I}V_{\text{out}}}{2} \frac{T_{\text{error}}(T_{\text{error}} - T_{\text{os}})}{T_{\text{fall}}} \quad (7)$$

where T_{fall} in this case is the ideal pFET on-time to achieve exact synchronization. If the pFET is turned off after the current has crossed zero, then the synchronization losses come from the output being discharged during the negative conduction time:

$$E_{\text{sync}} \approx \frac{\hat{I}V_{\text{out}}}{2} \frac{T_{\text{error}}^2}{T_{\text{fall}}} \quad (8)$$

TABLE I
ESTIMATED BREAKDOWN OF LOSSES (PERCENTAGE OF TOTAL LOSSES)
FROM SIMULATED DATA ($V_{\text{out}} = 1 \text{ V}$, $P_{\text{out}} = 10 \mu\text{W}$)

Source of Losses	$V_{\text{in}} = 25 \text{ mV}$	$V_{\text{in}} = 200 \text{ mV}$
Inductor series resistance	14.6%	3.4%
nFET gate driver	6.6%	12.4%
nFET channel resistance	29.2%	5.6%
pFET gate driver	2.8%	5.3%
pFET channel resistance	7.4%	16.6%
pFET synchronization error	3.3%	7.4%
V_D node capacitance	6.6%	12.3%
Static bias current	13.4%	33.1%
Control Logic	16.2%	3.9%

It can therefore be determined that overall efficiency is not sensitive to synchronization error, T_{error} . If the error is 20% of T_{fall} , then only 4% of the total output energy is lost.

Table I shows a breakdown of the boost converter losses estimated from simulation data for input voltages 25 mV and 200 mV. Losses due to resistance of the nFET and the inductor are more dominant in the 25 mV case because the nFET and inductor are conducting for a longer period of time for each switching cycle (T_{rise} is greater for $V_{\text{in}} = 25 \text{ mV}$) and therefore more energy is consumed per cycle. The pFET is on for the same amount of time for both cases (constant T_{fall}) and therefore the energy lost due to the pFET resistance is also constant. The control circuitry consumes significantly less power when the input voltage is 200 mV because T_{rise} is shorter and therefore it takes fewer clock cycles for the converter to complete one switching cycle.

B. Voltage Ripple

Besides efficiency, input and output voltage ripple must also be considered. The input voltage ripple is

$$\Delta V_{\text{in}} = \frac{E_{\text{in}}}{C_{\text{in}}V_{\text{in}}} \quad (9)$$

In general, C_{in} should be the largest capacitor possible in order to minimize input voltage ripple. A ripple voltage of 5% is considered sufficient for most applications (1 mV of ripple for a 20 mV input). A 2.0 mm \times 1.2 mm 10 μF input capacitor was used to achieve this requirement.

Likewise, the output voltage ripple is

$$\Delta V_{\text{out}} = \frac{E_{\text{out}}}{C_{\text{out}}V_{\text{out}}} \quad (10)$$

The requirements for the output voltage ripple are determined by what the load can tolerate. For our low power wireless sensing applications, 20 mV of ripple is considered sufficiently small, and is achieved with a 1.0 mm \times 0.5 mm 10 nF output capacitor.

C. Inductor

The inductor choice is critical for efficient boost converter operation. According to (4), a larger inductor value provides more

energy transfer per switching cycle (E_{out}). This improves efficiency because, as seen in (3), the constant gate drive losses become less significant compared to a larger output energy. Doubling the inductance effectively reduces the gate drive power losses by one-half because the converter only needs to switch half as often.

On the other hand, increasing the inductance generally comes at the expense of either physical size or parasitic series resistance. Doubling the inductance will nearly double the parasitic series resistance if the case size is kept constant [11]. The losses due to inductor series resistance are

$$E_{RL} = \frac{\hat{I}^2}{3} R_L (T_{\text{rise}} + T_{\text{fall}}). \quad (11)$$

We determined that a 4.7 μH inductor with $R_L = 230 \text{ m}\Omega$ and a 2.0 mm \times 2.0 mm footprint provides an appropriate tradeoff between resistive losses, switching losses, ripple, and area.

D. Power FETs

The losses of the power nFET and pFET are a tradeoff between conduction losses due to parasitic channel resistance and gate-drive losses due to parasitic gate capacitance. The gate-drive losses are proportional to the effective transistor width, while the channel resistance is inversely proportional to the transistor width. The conduction losses for the pFET and nFET are as follows:

$$E_{RN} = \frac{\hat{I}^2}{3} R_N T_{\text{rise}} \quad (12)$$

$$E_{RP} = \frac{\hat{I}^2}{3} R_p T_{\text{fall}}. \quad (13)$$

Because the gate drivers are powered from the boost converter's output, the effective losses are amplified by the efficiency of the converter:

$$E_{\text{gate-drive,eff}} = \frac{E_{\text{gate-drive}}}{E_{\text{out}}/E_{\text{in}}}. \quad (14)$$

An optimum efficiency tradeoff is achieved when the widths of the nFET and pFET are such that

$$\frac{d\eta}{dW} = 0 \quad (15)$$

where W is the width of either power FET device. The widths for the nFET and pFET were chosen to be 4.5 mm and 1.5 mm, respectively.

E. Peak Current Control

Section II stated that the peak inductor current \hat{I} was chosen to be the adjustable parameter to control T_{fall} such that it is equal to T_P , rather than directly adjusting T_P to match with T_{fall} . According to (6), for $V_{\text{in}} \ll V_{\text{out}}$, the peak inductor current \hat{I} is directly proportional to T_{fall} :

$$\hat{I} = T_{\text{fall}} \frac{V_{\text{out}} - V_{\text{in}}}{L} \approx T_{\text{fall}} \frac{V_{\text{out}}}{L} \approx T_P \frac{V_{\text{out}}}{L}. \quad (16)$$

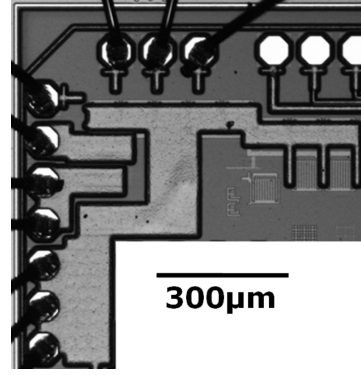


Fig. 9. Boost converter circuit micrograph.

While V_{out} and T_P are held constant, \hat{I} also remains relatively constant as long as $V_{\text{in}} \ll V_{\text{out}}$. It can be inferred from the prior efficiency analysis that keeping \hat{I} constant for varying V_{in} enables higher efficiency for low input voltages and reduces output voltage ripple for higher output voltages [12]. From (4) it is apparent that E_{out} is very sensitive to \hat{I} . If we were to use a control topology that keeps the nFET gate timing (T_{rise}) constant and adjusts the pFET gate timing (T_P) to achieve equal T_{fall} and T_P , then E_{out} would be approximately proportional to the square of the input voltage. The result would be almost zero transferred energy at very low input voltages and excessive output voltage ripple with higher input voltages. The peak current also limits the maximum average input current, which therefore limits the maximum output power:

$$E_{\text{load,max}} = \eta E_{\text{in,max}} = \eta \frac{\hat{I}}{2} V_{\text{in}} D \frac{T_{\text{rise}} + T_{\text{fall}}}{T_{\text{rise}}} \quad (17)$$

where D is the duty cycle of output of the oscillator block.

V. MEASURED RESULTS

The circuit was fabricated in a 0.13 μm CMOS process. Fig. 9 shows the die micrograph. The active area is: 35,000 μm^2 for the power FETs and gate drivers, 12,000 μm^2 for the control circuitry, and 70,000 μm^2 for output voltage filter capacitors. Parasitic resistance on the input and ground pins must be minimized. For example, 100 $\text{m}\Omega$ added in series with the inductor can degrade efficiency by 3%. To minimize this resistance, we use three pads for ground and two pads for the V_D node. The chip was assembled onto a PCB using chip-on-board wirebonding.

A. Waveforms

The output capacitor was initially precharged to 1 V and an input voltage of 50 mV was provided, and the converter was loaded with a 100 $\text{k}\Omega$ resistor (10 μW load). Fig. 10 shows the ripple of the output voltage (v_{out}) and the power FET drain voltage (v_D). The reference voltage V_{ref} was adjusted such that the average output voltage was exactly 1 V. The ripple voltage alternates between 10 mV and 15 mV due to the quantization of the frequency control circuit, which is continuously stepping up

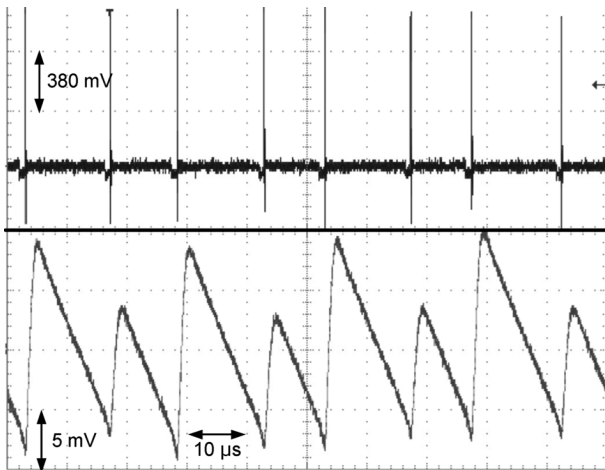


Fig. 10. Top: Power FET drain voltage (v_D). Bottom: Converter output voltage ripple (average voltage is 1 V).

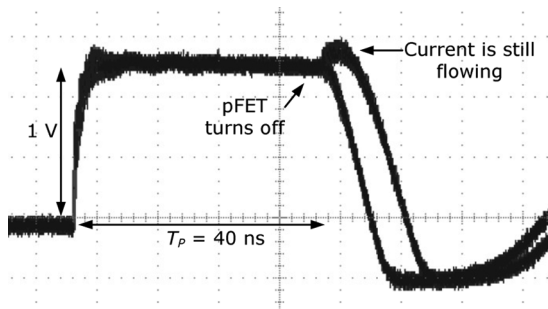


Fig. 11. Measured drain voltage waveform with persistence enabled. $V_{in} = 50$ mV, $V_{out} = 1$ V, $P_{load} = 10$ μ W.

and down to keep T_{fall} on average equal to T_P , as illustrated in Figs. 3 and 5.

Fig. 11 shows a close up view of the v_D voltage. The pFET on-time (T_P) can be inferred from the waveform to be about 40 ns. Persistence was enabled on the oscilloscope to show that T_{fall} cycles between two discrete values. For one cycle, v_D is high for about 5 ns longer than the other, and it can be seen that the drain voltage increases by about 200 mV toward the end of the conduction time because the current is still flowing after pFET is switched off.

B. Performance

The efficiency of the converter was measured for a variety of input voltages and loads. The results given in Fig. 12 show that the efficiency is somewhat flat for input voltages above 75 mV. In this range the efficiency is dominated by switching losses, which are mostly independent of input voltage. When the input voltage is below 75 mV, the efficiency becomes dominated by conduction losses, which become more prominent as the input voltage becomes closer to the voltage drops of the parasitic resistances. When the load power approaches the quiescent converter power, (roughly 1 μ W), the efficiency degrades significantly. The lowest input voltage where the boost converter can drive a 1 μ W load is 16 mV, with 13% efficiency. There is a sudden efficiency improvement when the input voltage is

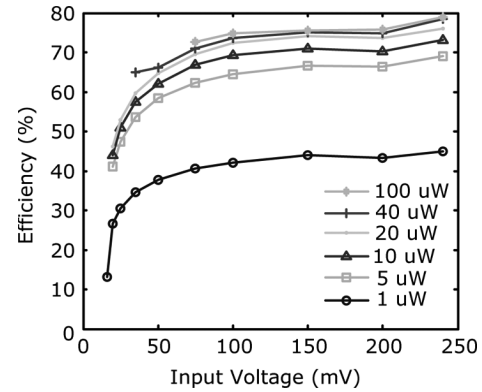


Fig. 12. Measured converter efficiency versus input voltage for different loads. $V_{out} = 1$ V.

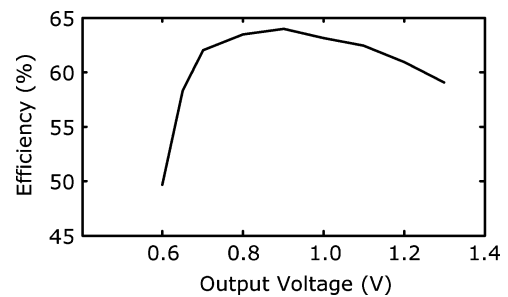


Fig. 13. Measured efficiency versus output voltage for $V_{in} = 50$ mV, $P_{load} = 10$ μ W.

240 mV because at this voltage the counter in the frequency control circuit has saturated high and T_{fall} does not change between cycles.

Fig. 13 shows the efficiency versus the output voltage for a 50 mV input and a 10 μ W load. The converter is most efficient when the output voltage is 0.9 V, while the efficiency quickly degrades as the output voltage drops below 0.7 V. The efficiency reduction at low output voltages is primarily due to the increased switch resistances resulting from less voltage applied to the FET gates, while the efficiency reduction at higher voltages is due to the increase in energy required to drive the FET gates and the control logic.

Table II provides a summary of the boost converter performance. Unloaded, the boost converter can operate in input voltages down to 15 mV before the losses become too great to sustain a voltage at the output. Although the converter will function with input voltages above 250 mV, the frequency control circuit saturates beyond this point and the gate-timing synchronization feedback mechanism ceases to function properly. The converter supports output voltages up to 1.4 V: voltages beyond this exceed the voltage ratings of the transistors. If the output voltage drops below 600 mV, the power FETs can no longer be sufficiently switched on, and the converter will not function.

C. Comparison With Prior Work

To the best of the authors' knowledge, this paper reports the highest efficiency 20 mV input boost converter to date. Ref. [13] reports 20 mV to 3.4 V conversion, but an "average" efficiency of 30%. Other low power and low voltage step-up converters

TABLE II
BOOST CONVERTER PERFORMANCE SUMMARY

Source of Losses	$V_{in} = 25 \text{ mV}$	$V_{in} = 200 \text{ mV}$
Inductor series resistance	14.6%	3.4%
nFET gate driver	6.6%	12.4%
nFET channel resistance	29.2%	5.6%
pFET gate driver	2.8%	5.3%
pFET channel resistance	7.4%	16.6%
pFET synchronization error	3.3%	7.4%
V_D node capacitance	6.6%	12.3%
Static bias current	13.4%	33.1%
Control Logic	16.2%	3.9%

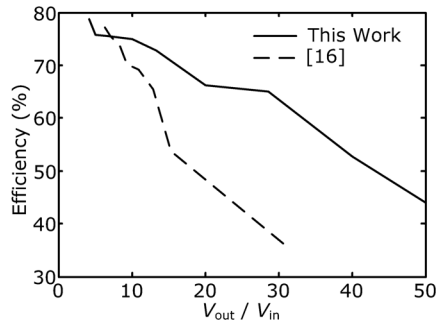


Fig. 14. Efficiency comparison between this work ($V_{out} = 1 \text{ V}$) and [16] ($V_{out} = 4.2 \text{ V}$).

typically operate either with much higher quiescent power consumption [14], or have low step-up ratios [15]. Ref. [16] is the only work that we have seen that achieves efficient operation for a conversion ratio greater than 10 and load power on the order of $10 \mu\text{W}$ with sufficient data for comparison. Fig. 14 compares the efficiency results with those achieved in [16]. Because [16] operates with higher output voltages (4.15 V), results are compared normalized to voltage conversion ratios. It can be seen that for conversion ratios above 8, this work achieves significantly greater efficiency, which can be attributed to low quiescent power consumption and optimum device size selection. The circuit in [16] does not suffer from severe losses from the high-side diode voltage drop because the output voltage is much higher than the voltage drop.

D. Characterization With a Thermoelectric Generator

We have performed some initial characterization of the boost circuit connected to a 1 cm^2 thermoelectric generator. The TEG has an internal resistance of 3.9Ω . Fig. 15 shows the maximum power that could be extracted from the TEG given an applied temperature. The temperature is given relative to ambient temperature (24°C). A 4°C temperature differential is required to get the $\sim 20 \text{ mV}$ input voltage required for efficient operation. The circuit was then tested with body heat from a human arm. The converter was allowed to reach thermal equilibrium over a period of 10 minutes. At equilibrium, the generator produced 34 mV (unloaded voltage) and the boost converter was able to deliver $34 \mu\text{W}$ at 1 V .

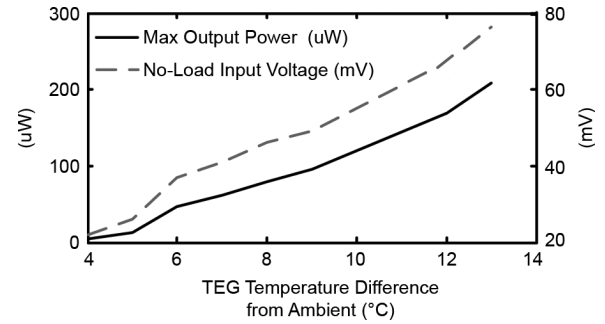


Fig. 15. The unloaded (open circuit) voltage generated by the TEG and the maximum power deliverable at 1 V versus the temperature difference of the hot side of the TEG from ambient (ambient temperature is 24°C).

VI. CONCLUSION

Many emerging energy-harvesting power sources such as TEGs fail to provide the voltages needed for low power wireless sensors. We have demonstrated that a switched-mode DC-DC boost converter can efficiently generate a 1 V output from input voltages as low as 20 mV . A novel control circuit uses peak current regulation to allow efficient operation for input voltages ranging between 20 mV and 250 mV , while consuming less than $2 \mu\text{W}$ of quiescent power. The control circuit includes a load control feature that disables the load when input voltages become critically low. It was also shown that the conversion efficiency from this work is significantly greater than that found in prior work for high conversion ratio low power boost converters.

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