25.9 A 1.6mW 300mV-Supply 2.4GHz Receiver with -94dBm Sensitivity for Energy-Harvesting Applications

Fan Zhang[1], Keping Wang[1], Jabeom Koo[1], Yasunori Miyahara[2], Brian Otis[1]

[1]University of Washington, Seattle, WA, [2]Panasonic, Yokohama, Japan

Low power, short-range ISM band transceivers have become extremely important in enabling new applications and have become highly successful commercially. New energy harvesting methodologies will open further applications but demand lower power and supply voltages than currently available chipsets can provide. For example, on-chip solar cells allow only a 200mV to 900mV supply; thermoelectric generators can be used for on-body generation, but provide low supply voltages (50-300mV) [1]. Although boost converters can be employed, their limited efficiency (40%~75%) often incurs a significant power penalty [2].

The goal of this work was to design a 2.4GHz receiver that operates with a supply voltage of 300mV, allowing direct powering from various energy-harvesting sources. Our target application is body-worn wireless devices requiring high datarates (wirelessly tethered hearing aids, for example). This application allows access to multiple energy-harvesting power sources, like photovoltaic and thermoelectric power harvested from body heat.

Our receiver uses the following techniques to allow operation from a 300mV supply. First, we extensively utilize transformer coupling between stages to reduce headroom requirements. This strategy also allows inter-stage impedance transformation and single-ended-to-differential conversion. The entire front-end comprises single-stack nFETs with $V_{ds} = V_{dd}$, maximizing utilization of the 300mV supply. Secondly, we use forward-biased bulk-source junctions to lower threshold voltages where appropriate. Thirdly, biasing key transistors in the RF signal path in moderate inversion optimizes the trade-off between power consumption and f_t.

Figure 25.9.1 shows the proposed architecture. A single-ended 2.4GHz RF input is amplified and converted to a differential signal before downconverting to a low-IF of 1 to10MHz. IF amplifiers and narrowband filters are interleaved to perform programmable channel selection. We use an interleaved planar bifilar topology for the transformers to achieve a 6nH inductance with a coupling coefficient k of 0.82 and a Q of 12.6 measured at 2.4GHz.

Figure 25.9.2 shows the RF front-end. We use a folded-cascode LNA topology to reduce headroom requirements while achieving high LNA gain and reverse isolation. Unlike previous folded-cascode LNA structures [3], we use transformer coupling instead of a pFET to eliminate voltage overhead and realize an intrinsic balun. By forward-biasing the bulk-source junction voltage of the three nFETs by 300mV, we lower their threshold voltage by 10%. This allows us to bias the transistors in moderate inversion, increasing their current efficiency (g_m/I_d) and normalized f_t/f_0 product by 100 to 200% compared to a weak-inversion operation. Compared to their pFET counterparts, the lower impedance and smaller parasitic capacitance looking into the source of the nFET cascode transistors improves the linearity, lowers the noise contribution from the cascode device, and provide better reverse isolation. To further lower the source impedance of the cascode transistors, we used capacitive-coupled g_m-boosting in the 2nd LNA stage.

To maximize swing under a low supply voltage, we employed a transformer-feedback VCO. Phase noise is further reduced by two mechanisms. First, coupled transformers exhibit larger effective inductance per area and better quality factor compared to a single inductor. Secondly, transformer feedback across the drain and source nodes improves the cyclo-stationary noise property, similar to the Colpitts/Hartley design.

Conventional Gilbert-cell mixers require two or more transistors stacked, resulting in a higher supply voltage. Alternatively, we used a double-balanced passive mixer that requires no stacked transistors and exhibits lower 1/f noise and higher linearity. We transformer-couple the VCO to the source instead of the conventional mixer gate to avoid loading the LNA output tank with the upconverted load impedance of the mixer.

Figure 25.9.3 shows the schematic of the IF-chain. Due to the severe headroom limitation, we used two single-ended self-biased inverters instead of OTAs as IF amplifiers. Compared to a conventional common-source stage, this current-reuse topology that amplifies using both the nFET and pFET doubles the transconductance and gain for the same bias current. Two stages of fully-differential gain provide common-mode rejection and attenuate the input-referred offset voltage of the IF chain to negligible levels. A chain of inverters completes the limiting amplifier and provides a rail-to-rail output.

Conventional IF filters employ g_m-C or OTAs, which are extremely challenging under a 300mV supply. Here we propose using a passive frequency-translated filter to perform channel selection. The principle is predominantly used in RF front-ends [4]. An 8-phase clock drives switches and transforms the lowpass response at DC to a high-Q bandpass response at IF. A Johnson-counter generates 8 phases with 1/8 duty cycle from a single clock source that runs at 8 times the IF frequency. We forward bias the bulk-source junction of the switches to lower their turn-on voltage. Because switches still require a voltage higher than 300mV to fully turn on, we used an on-chip level shifter to convert the switch gate voltage to 600mV. Figure 25.9.4 shows the normalized response of the full receiver with the filters turned on. We achieve a steep channel select filtering of 12dB and 30dB at 1MHz offset with one and two filters on, respectively.

Figure 25.9.5 shows the measured receiver performance. The LNA achieves a 4.7dB noise figure (NF) with 20.2dB of gain at 2.46GHz. At the IF amplifier output, we measure a conversion gain of 83dB and a total DSB NF of 6.1dB at a 6MHz IF. We achieve an IIP3 of -21.5dBm at the mixer output. We injection-lock the VCO with an external source to characterize the performance. In practice, a PLL can be used to lock the VCO. The transformer-coupled VCO is able to achieve -112.8 and -140dBc/Hz at 1MHz when free-run and locked respectively.

The chip was fabricated in a 65nm CMOS process. Our chip operates from a single 300mV supply while dissipating 1.6mW. Based on the SNR requirement of the Zigbee standard (7dB SNR at the demodulator for a 2MHz channel bandwidth), this receiver achieves -94dBm sensitivity. When input with a BFSK signal at 200kb/s modulated with a pseudo-random number sequence, we achieved a sensitivity of -91.5dBm for a BER of 10e-3 (this is consistent with theory given the 3dB advantage of QPSK over BFSK). A performance summary and comparison with the state-of-the-art is presented in Fig. 25.9.6. This radio allows a lower supply voltage and achieves higher total gain than the other GHz-range radios shown in Fig. 25.9.6.

Acknowledgement:
We acknowledge Dominik Eyerly and Jingren Gu for their valuable contributions.

References:
[1] S. Bandyopadhyay, et al., "Platform Architecture for Solar, Thermal, and Vibration Energy Combining with MPPT and Single Inductor", *IEEE J. Solid-State Circuits*, vol. 47,no. 9, pp. 2199-2215, Sep 2012.
[2] E.J. Carlson, et al., "A 20 mV Input Boost Converter with Efficient Digital Control for Thermoelectric Energy Harvesting," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 741-750, Apr. 2010.
[3] D. Linten, et al., "Low-Power 5 GHz LNA and VCO in 90 nm RF CMOS", *IEEE Symp. VLSI Technology*, pp. 372-375, June 2004.
[4] A. Mirzaei, et al., "A Low-Power Process-Scalable Superheterodyne Receiver with Integrated High-Q Filters", *ISSCC Dig. Tech. Papers*, pp.60-61, Feb. 2011.
[5] A. Balankutty, et al., "A 0.6-V Zero-IF/Low-IF Receiver With Integrated Fractional-N Synthesizer for 2.4-GHz ISM-Band Applications", *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 538-553, Mar. 2010.
[6] B. Cook, et al., "Low-Power 2.4-GHz Transceiver With Passive RX Front-End and 400-mV Supply", *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2757-2766, Dec. 2006.
[7] M. Brandolini, et al., "A 750 mV Fully Integrated Direct Conversion Receiver Front-End for GSM in 90-nm CMOS", *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp.1310-1317, June 2007.
[8] H. Chen, et al., "0.5-V 5.6-GHz CMOS Receiver Subsystem", *IEEE Trans. Microwave Theory and Techniques*, vol. 47, no. 2, pp. 329-335, Feb. 2009.

 978-1-4673-4516-3/13/$31.00

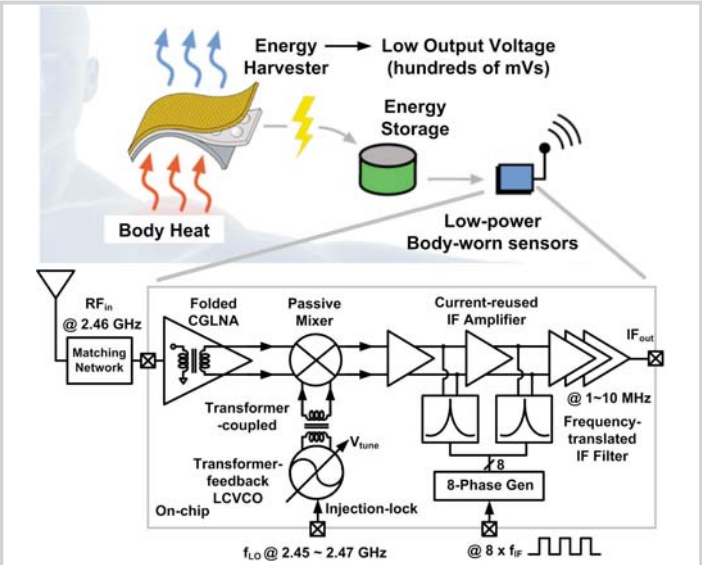

Figure 25.9.1: Proposed system block diagram.

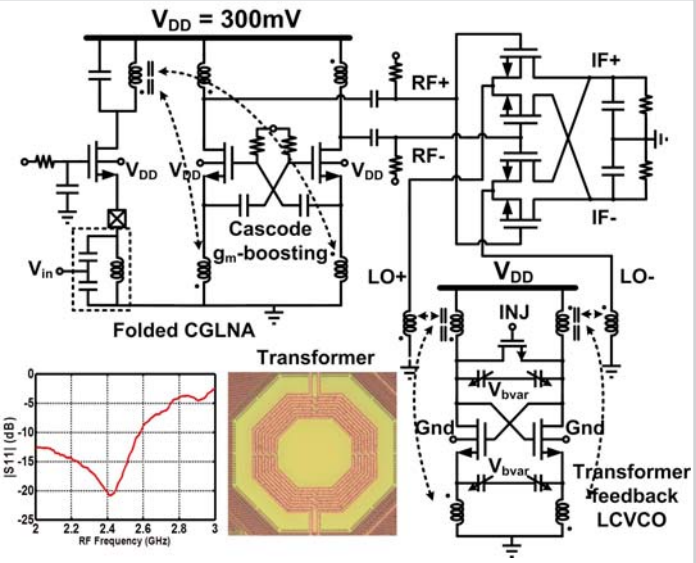

Figure 25.9.2: RF front-end (LNA, VCO, mixer) schematic (bias not shown).

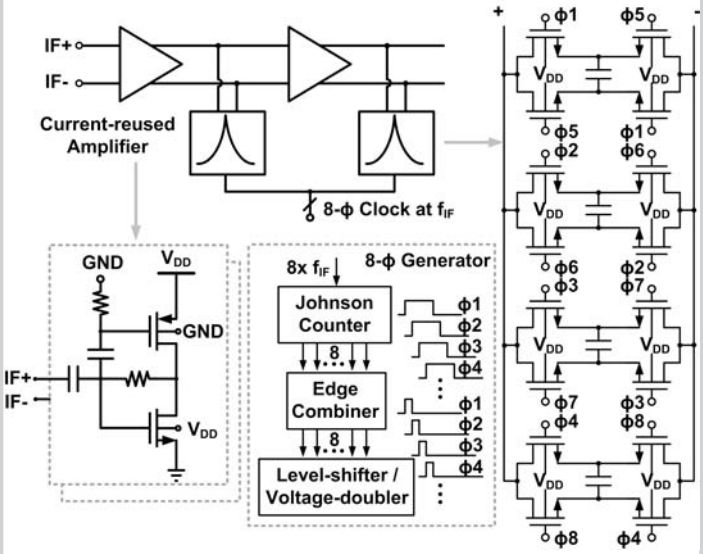

Figure 25.9.3: IF amplifier and frequency-translated filter schematic.

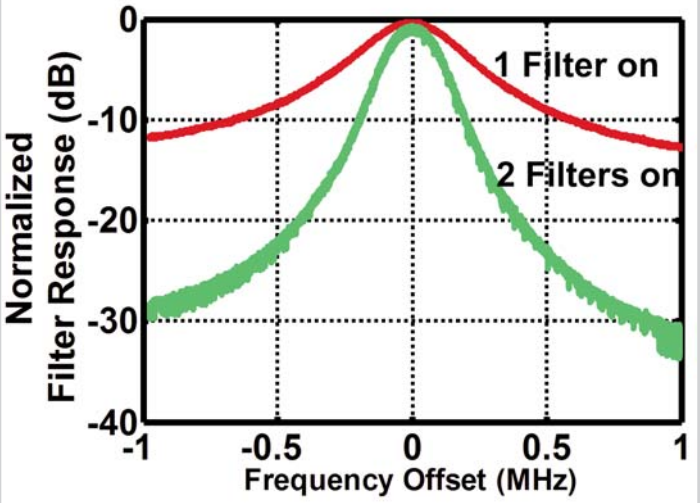

Figure 25.9.4: Measured IF frequency-translated filter response (normalized).

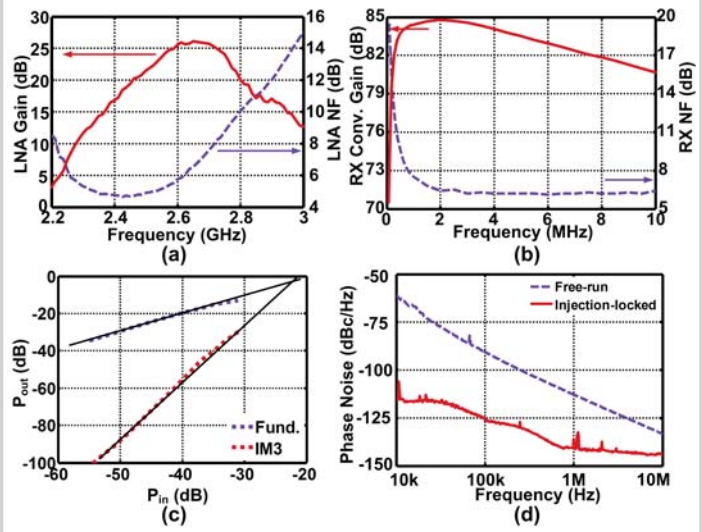

Figure 25.9.5: (a) LNA gain and NF; (b) receiver conversion gain and NF; (c) front-end IIP3; (d) VCO phase noise.

Performance Comparison					
	This Work	[5]'10 JSSC	[6]'06 JSSC	[7]'07 JSSC	[8]'09 MTT
Supply voltage [V]	0.3	0.6	0.4	0.75	0.5
Power Consumption [mW]	1.6	32.5	0.33	11.3	26.2
RF Input Frequency [MHz]	2460	2400	2340	1950	5600
Voltage Gain [dB]	83	67	NA	31.5	27.1
NF [dB]	6.1	16	7	3.5	8.6
IIP3 [dBm]	-21.5	-10.5	-7.5	-10.5	-17.9
LO Phase Noise [dBc/Hz] @ 1MHz offset	-112	-115	-106	NA	NA
Technology	65nm CMOS	90nm CMOS	130nm CMOS	90nm CMOS	180nm CMOS
Area [mm^2]	2.496	2.9	4.4	4.3	NA

Performance Summary			
@ the output of	LNA	Mixer	IF Amp
Total Gain [dB]	20.2	20.7	83
Total NF [dB]	4.7	5.1	6.1
Total IIP3 [dB]	-20	-21.5	-
Stop-band Rejection [dB] @1MHz offset	12 (1 filter on)	30 (2 filters on)	
LO Phase Noise (locked) [dBc/Hz]	-115@10kHz	-126@100kHz	-140@1MHz
LO Phase Noise (free-run) [dBc/Hz]	-61@10kHz	-90.8@100kHz	-112.8@1MHz

Power Breakdown [mW]						
LNA	Mixer	VCO	IF Amps	IF (Dig)	8-Phase Gen	Total
0.93	0	0.6	0.046	0.015	0.005	1.596

Figure 25.9.6: Performance summary and comparison.

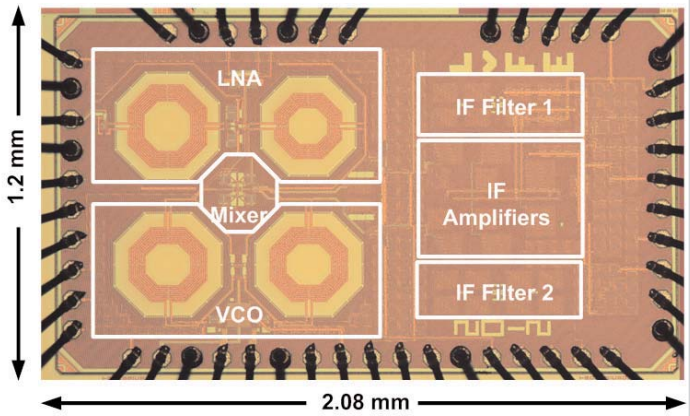

Figure 25.9.7: Die micrograph.

978-1-4673-4516-3/13/$31.00