A 22μW, 2.0GHz FBAR Oscillator

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***Abstract*—We present a 22μW, 2.0GHz FBAR oscillator - the lowest power reported to date for a GHz-range oscillator of this type. Low power consumption is achieved through co-design with a high R_p FBAR resonator and a weakly-forward biased bulk connection. An oscillator with a standard bulk connection was fabricated for comparison. The chip was fabricated in a 0.18μm CMOS process. The weakly-forward biased bulk led to a 41% reduction in power dissipation. The measured phase noise is -121dBc/Hz at a 100kHz offset.**

***Index Terms*—Film bulk acoustic resonators, Oscillators, Voltage-controlled oscillators, Phase noise, Low voltage.**

I. Introduction

Over the past ten years, FBAR-based filters have demonstrated their ability to provide steep low loss miniaturized filtering, and are currently deployed in billions of mobile phones. The individual resonators used in these filters have been increasingly applied to active circuitry. Their high quality factors, small size, high power handing capability, and tight frequency tolerance make them compelling for oscillator and frequency synthesizer design [1][2].

These resonators operate in the GHz range, making them suitable for use in wireless RF systems or, when divided down to the MHz-range, as frequency references. In low power RF oscillator design, the power consumption is determined by the magnitude of the tank impedance at resonance. Unlike an LC tank, the Q of an FBAR resonator is not directly linked to its impedance at the parallel resonance (R_p). Historically, the R_p of FBAR resonators has been in the 1kΩ to 2kΩ range. The negative resistance needed for oscillation is derived from the device transconductance (g_m). Assuming a MOSFET biased in the moderate inversion region yields a g_m/I_d of approximately 20, the bias current required for an FBAR Pierce oscillator startup is roughly $0.4/R_p$ for an initial loop gain of 2. Thus, the first published FBAR oscillators consumed between 200-300μA [1][2][3]. For ultra-low power applications like data transceivers or quartz reference replacement, extremely low power operation is necessary (below 50μW). It follows from this discussion that there are two ways to reduce the power consumption of an FBAR oscillator:

1) Increase the impedance of the resonator at resonance (R_p) to reduce the necessary g_m (and thus bias current)
2) Reduce the supply voltage

In this paper, we present advances in both of these techniques to demonstrate the lowest power consumption for an FBAR oscillator reported to date. In Section II of this paper, we provide details about our high R_p FBAR resonator and our low Vdd oscillator design. In Section IV, we provide measured results from two prototype circuits.

II. The proposed FBAR oscillator architecture

The proposed low power FBAR oscillator is shown in Fig. 1. A pFET current mirror provides bias current to the Pierce oscillator. The oscillator uses an AC-coupled open drain buffer to carry the oscillator signal off-chip. There are two distinct characteristics that allow the oscillator to operate at extremely low power: a high R_p FBAR and a weakly forward-biased bulk (FBB). The following two subsections will elaborate these two characteristics.

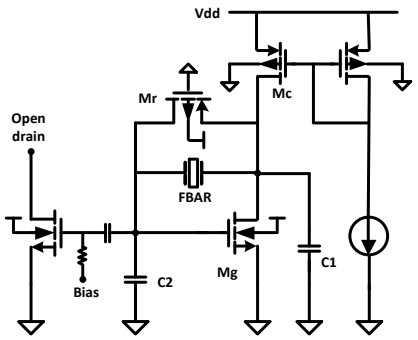

Fig. 1. Schematic of the proposed low power FBAR oscillator with weakly forward biased bulk (FBB).

A. High resonator impedance R_p

As shown in Fig. 1, a transformer comprised of capacitors C1 and C2 senses the output voltage of the FBAR tank. The transconductor Mg uses the feedback voltage across C2 to generate a current. This current is injected into the FBAR tank to excite an output voltage and forms a positive feedback loop. The equivalent circuit for the Pierce oscillator core is shown in Fig. 2. It shows that the negative resistance resulting from transistor Mg is proportional to transconductance g_m. To achieve oscillation, transistor Mg must exhibit a sufficent g_m to compensate for the energy loss occurring within the FBAR resonator (and other losses in the circuit) to sustain oscillation.

The FBAR is fabricated in a planar silicon process. Fig. 3 shows a simplified cross-sectional view of the FBAR device. It consists of a minimum of three layers: two metal electrode layers surrounding one piezoelectric layer. The two-terminal structure generally consumes a silicon area of roughly 100x100μm^2.

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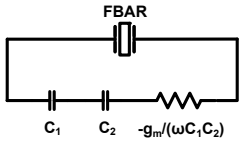

Fig. 2. The equivalent circuit of the oscillator core.

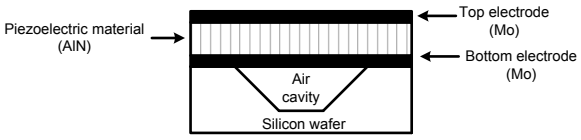

Fig. 3. Simplified cross-sectional view of an FBAR device.

An FBAR has a series resonance f_s and a parallel resonance f_p at hundreds of MHz to several GHz with quality factors larger than 2000 (Fig. 4). The resonant frequency f_s is determined by the thickness of the layers that compose the FBAR. The parallel resonance f_p is influenced by the proportion of thickness of the electrodes (Mo) and the piezoelectric material (AlN) [4]. Parameters that affect an FBAR oscillator performance include: kt^2, a measure for frequency separation between f_s and f_p; quality factor; R_p, the impedance of the tank at frequency f_p; and R_s, the impedance of the tank at frequency f_s. To realize a wide tuning range FBAR oscillator, a large kt^2 is desirable. However, a large kt^2 generally implies a reduced quality factor of the resonator and hence increased oscillator phase noise.

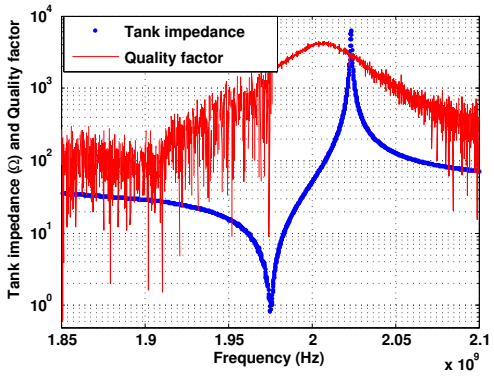

Fig. 4. Measured tank impedance and the quality factor vs. frequency of a high R_p FBAR.

The proposed FBAR oscillator operates at parellel resonance f_p. The tank impedance R_p generally falls at around 1-2kΩ. As Fig. 2 indicates, this requires a large g_m from the transconductance transistor Mg to provide a relatively large negative resistance to compensate for the resistive loss. In order to achieve low power consumption, R_p is increased through FBAR process optimization. Fig. 4 shows the measured FBAR characteristic. R_p can be maximally increased with acceptable degradation of the quality factor at increased kt^2. The measured impedance R_p is as high as 7kΩ, the quality factor is 3000, and kt^2 is 5.6%.

B. Forward biasing of transistor bulks

Increasing R_p of the FBAR tank can effectively reduce the bias current of the transconductance transistor Mg. To further reduce power consumption, we can reduce the power supply voltage Vdd. Analog circuitry typically suffers greatly under reduced Vdd values. Linear amplifiers, for example, which encode information as a voltage, suffer a significant reduction in dynamic range when the supply voltage is reduced. Oscillators, however, encode their signal in the time (frequency) domain. Thus, with the high Q tank provided by the FBAR resonator, extremely good phase noise can be achieved even with reduced oscillator swings and supply voltages. In this situation, the threshold voltage of the transistor starts to limit the achievable reduction in oscillator supply voltage. Fig. 5 shows the structure of a triple well NMOS transistor available in our 0.18μm CMOS process. In a traditional biasing condition, the bulk terminal (B) is connected to the lowest voltage (ground in most cases) to ensure unconditional reverse biasing between the bulk and the source/drain.

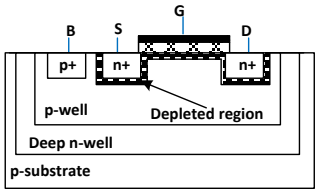

Fig. 5. Cross-sectional view of a triple-well nFET.

In this design, we weakly forward-bias the bulk terminal of PMOS and NMOS transistors using the ground and supply voltage (Vdd), respectively. If Vdd is kept low (below 0.5V or so), the resulting forward-bias current in the bulk/source diode is negligible. The threshold voltage of a NMOS transistor to first order is given by:

$$V_{th} = \phi_{MS} + 2\phi_F + \frac{Q_{dep}}{C_{ox}}, \quad (1)$$

where ϕ_{MS} is difference between the work function of the gate and the substrate, and ϕ_F is the potential built up by the pn-junction itself, Q_{dep} is the amount of charge in the depletion region. Forward-biasing the bulk terminal effectively reduces the amount of charge in the depletion region, thus reducing the threshold voltage. Fig. 6 shows the simulation results for a typical nFET V_{th} at different bulk-to-source bias voltage V_{BS}. The threshold voltage reduces by 220mV when V_{BS} is increased from -0.5 to 0.5V and by 100mV from 0 to 0.5V. With a reduced threshold voltage, we are able to achieve increased transconductance for a given suppy voltage, saving power without further increasing device size (and thus parasitic capacitance).

To demonstrate the effectiveness of power saving using forward-bulk biasing technique, we have designed a version of the same oscillator with all the transistors using a standard

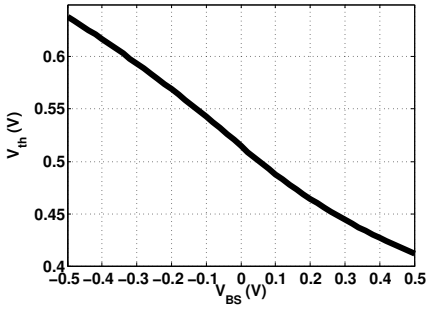

Fig. 6. Simulated threshold voltage of a typical nFET as a function of bulk-to-source voltage.

bulk bias (SBB). The schematic is shown in Fig. 7. Fig. 8 shows the simulated oscillator loop gain versus the supply

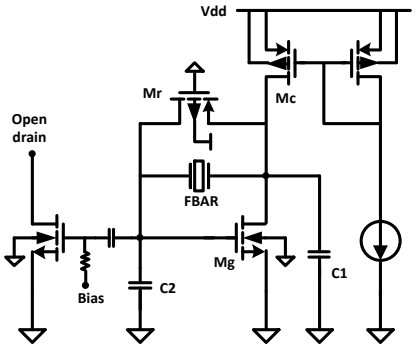

Fig. 7. The schematic of the FBAR oscillator with standard bulk bias (SBB) for comparison.

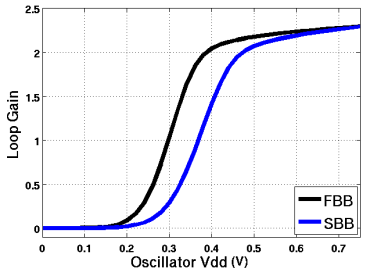

Fig. 8. Simulated loop gain versus supply voltage for both forward and standard bulk biased oscillators.

voltage Vdd. The plot shows that the proposed forward bulk bias scheme reducing the required Vdd by 100mV to achieve the same oscillator loop gain.

III. Design Issues

The oscillator needs to be carefully biased and sized to avoid as per the following:

1. Any resistive load across the FBAR tank from the CMOS circuitry needs to be significantly larger than the R_p to minimize Q degradation. This includes transistor output resistance and the feedback resistor Mr. Resistive loading is particularly sinister since it reduces the effective R_p (requiring a higher g_m) while simultaneously reducing the resonator Q (dramatically hurting the phase noise performance).

2. Any capacitive load across the FBAR tank pulls the parallel resonant frequency downward and reduces the resonator R_p. This reduction in R_p causes an increase in the necessary power consumption but does not necessarily reduce the FBAR Q.

We bias the oscillator by sythesizing a large resistor using a PMOS transistor working in linear region. Transistors Mg and Mc need to be sized to operate with extremely low g_{ds}.

To maintain a high R_p, i.e., low power operation, capacitive loading to the FBAR tank has to be minimized. The transformer capacitors C1 and C2, comprise parasitic capacitance provided by the FBAR pads and the transistors. An explicit capacitor of 100fF is added to C1 to balance the capacitance of C1 and C2. This balances the oscillator voltage swing and provides an optimal startup condition.

The transconductance efficiency (g_m/I_d) is increased by operating the oscillator in moderate inversion (g_m/I_d= 23). An optimal device size exists for minimum current consumption: increasing the width of Mg can further increase g_m/I_d, but cause a significant reduction in R_p due to the increase in parasitic capacitance.

IV. Results

The design was fabricated in a 0.18μm CMOS process and has an active area of 130×60μm^2. A die photo is shown in Figure 9. The FBAR is epoxied directly on top of the CMOS

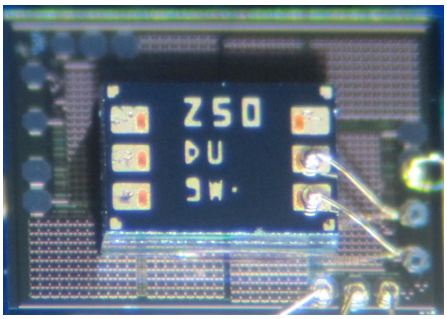

Fig. 9. Die photograph showing FBAR resonator stacked on the CMOS die. This photo shows the FBAR bonded to the FBB oscillator. The SBB oscillator is visible on the left side of the CMOS die with a padring symmetric to the FBB die.

chip. Gold ball bonds connect the resonator terminals to the oscillator.

Fig. 10 is a measurement plot showing the minimum power required for oscillation at various supply voltages for the FBAR oscillator (FBB) in comparison with that of the standard bulk-biased design (SBB). The FBB oscillator achieves reliable startup at a power level of 22μW, which occurs at Vdd of 340mV. For the SBB version, the minimum power is 31μW at Vdd of 490mV. While the SBB version consumes nearly constant current as the voltage is raised above 500mV,

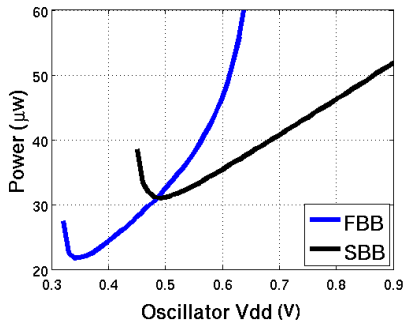

Fig. 10. Measured power comsumption vs. supply voltage for both oscillators.

the FBB version shows an exponential increase in current due to the bulk diode turning on. This indicates that forward-bulk biasing is a reasonable choice for low power in low supply voltages. For supply voltages less than 500mV, the leakage current in the bulk/source diode is negligible.

The measured frequency spectrum of the low power FBAR oscillator is shown in Fig. 11. The oscillator operates at

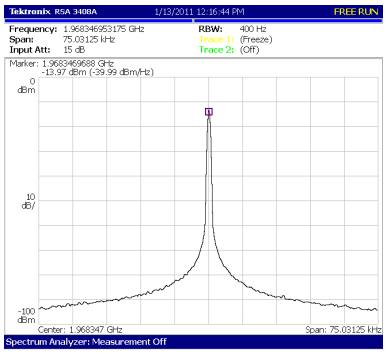

Fig. 11. The measured frequency spectrum of the low power FBAR oscillator.

2.0GHz. The output swing of the oscillator is around 100mV peak-to-peak.

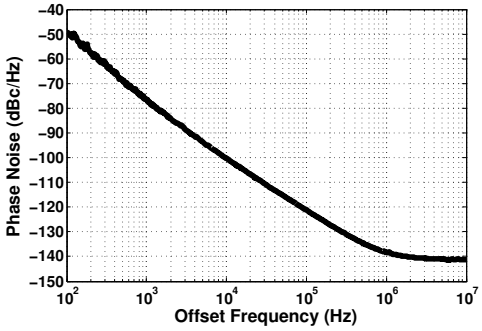

Fig. 12. The measured phase noise of the low power FBAR oscillator.

Table I
PERFORMANCE COMPARISON OF THE LOW POWER FBAR OSCILLATOR TO PREVIOUSLY PUBLISHED WORK.

Ref.	f_{OSC} (GHz)	Power (μW)	Current (μA)	Phase Noise @ 100kHz offset	FOM (dB)
This work	2.0	25	72	-121 dBc/Hz	222.9
[1]	1.9	300	300	-120 dBc/Hz	210.8
[2]	2.1	600	600	-122 dBc/Hz	212.1
[3]	1.9	104	206	-122 dBc/Hz	217.4
[5]	0.6	5600	44800	-140 dBc/Hz	208.1

The measured phase noise is shown in Fig. 12. The measurement is taken when the oscillator is operating at 350mV and 25μW with an Agilent E5052B Signal Source Analyzer. The measured phase noise is -121dBc/Hz at frequency offset of 100kHz.

Table I shows the performance of the low power FBAR oscillator compared to other published FBAR oscillators. We use equation

$$FOM = 10\log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L(\Delta f)\times P_{diss}/mW}\right] \quad (2)$$

for the oscillator figure-of-merit (FOM) calculation. This work achieves the highest FOM reported to date.

V. CONCLUSION

This paper presents the lowest power FBAR-based oscillator reported to date. Two techniques were used to achieve low levels of power dissipation. First, the circuit was co-designed with a high-R_p FBAR resonator to reduce the required bias current. Secondly, a weakly forward bulk bias (FBB) was used to allow a significant reduction in supply voltage. These two techniques yield a power dissipation of 22μW, 41% lower compared to a reference design without FBB. The oscillator operates at 2.0GHz with a phase noise of -121dBc/Hz at 100kHz offset, allowing the best reported RF oscillator figure of merit of 222.9.

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