# A 50ppm 600MHz Frequency Reference Utilizing the Series Resonance of an FBAR

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***Abstract*—A 600MHz thin film bulk-acoustic wave resonator (FBAR)-based differential oscillator fabricated in a 0.13$\mu$m CMOS process is presented. The oscillator employs a cross-coupled pair with an FBAR resonator tank providing high Q source degeneration to realize frequency oscillation at the series resonance. The measured phase noise is -126 and -150dBc/Hz at 10kHz and 1MHz frequency offsets respectively; the integrated RMS jitter from 10kHz to 20MHz is 50fs. The oscillator achieves a frequency drift of 50ppm over the temperature range from 25 to 110 °C, providing the potential for quartz replacement in some applications. The figure-of-merit (FOM) of the oscillator is 214dB.**

## I. Introduction

Thin film bulk-acoustic wave resonators (FBARs) have become critical building blocks for miniaturizing mobile phone transceivers. The need for high quality factor (Q) RF duplexers and filters has driven the FBAR manufacturing process to maturity; this includes well-controlled resonator frequency, quality factor, and temperature dependence with continued cost and size reduction [1].

FBAR-based oscillators have demonstrated superb phase noise performance due to their high Qs (>2000) [2][3]. An uncompensated FBAR resonator is sensitive to temperature variation with a temperature coefficient (TC) of about -25ppm/$^o$C [4]. Physical compensation, wherein a layer of positive TC material is added to the FBAR stack to cancel the TC of the piezoelectric material in the first order, significantly reduces its TC. Further electronic temperature compensation can be be implemented as in [5].

As the size of the resonator (typically 100×100$\mu$m$^2$) shrinks, the Q near the parallel resonance becomes poor. In contrast, Q near series resonance is less sensitive to shrinking area. Therefore, further size reduction of the resonator requires the oscillator to operate near the series resonance to utilize the maximal Q and maintain the phase noise performance. The motivation for this work is to present an efficient oscillator topology allowing operation near the series resonance of an FBAR.

Few previous works on series FBAR/BAW oscillators have been reported. Work in [6] demonstrated a series FBAR resonator in a SiGe BiCMOS process which achieved an inconsistent phase noise performance over a tuning range of 1.2% at a large power consumption.

This paper presents a CMOS differential oscillator that operates near the series resonance of an FBAR resonator (Fig. 1). Section I introduces the proposed oscillator. Section II discusses design challenges and proposes solutions. Section III presents the test results of our prototype.

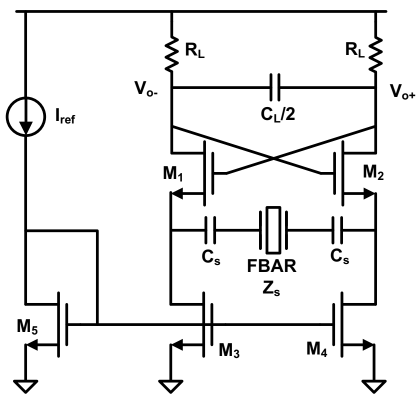


Fig. 1. The proposed FBAR oscillator operating at the series resonance.

## II. The proposed FBAR series oscillator

FBAR resonators are fabricated in a planar process which involves a minimum of three layers on a silicon substrate: two metal electrode layers surrounding one piezoelectric layer. The electrical behavior near the resonances can be accurately modeled using a modified Butterworth Van-Dyke (mBVD) model (Fig. 2). At the series resonance $f_s$, the resonator tank impedance reaches the minimum value $R_s$ (several Ω), and at parallel resonance $f_p$, it reaches the maximum value $R_p$ ($>$ 2000Ω). At both high and low frequencies, the resonator behaves capacitively. The maximum Q value ($>$ 2000) of the resonator appears at a frequency between the two resonances. The FBAR tank characteristic is modified by the additional impedance presented by the oscillator circuitry. A parallel capacitor $C_p$ across the tank pulls the parallel resonance $f_p$ and the maximum impedance $R_p$ to a lower value. Likewise, a capacitor $C_s$ in series with the tank pushes the series resonance $f_s$ and the minimum tank impedance value $R_s$ to a higher value. We will use this property to manipulate the series impedance of the FBAR, allowing efficient series-mode oscillation.

Like most LC oscillators, parallel resonance-mode FBAR oscillators drive the resonator tank with a current and sense the return voltage from the tank to the input of a transconductor. In contrast, a series oscillator drives the resonator with a voltage and senses the current. Using duality, a straightforward oscillator implementation operating at the series resonance of

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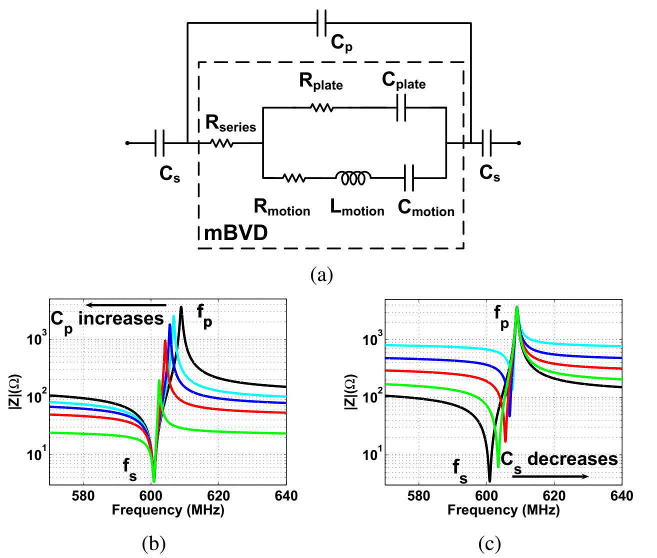


Fig. 2. FBAR characteristic. (a) The mBVD model with load capacitors. (b) Impact of parallel load $C_p$ on frequency response. (c) Impact of series load $C_s$ on frequency response.

the impedance tank is shown in Fig. 3 [6]. This oscillator uses a source follower to isolate the gain stage, which degrades power efficiency. We propose a new differential series oscillator topology that uses two-stage amplification realized with cross-coupled devices (Fig. 1). The equivalent circuit of our

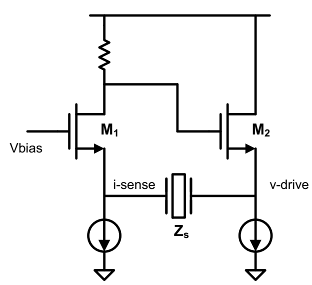


Fig. 3. Traditional implementation of series oscillators.

proposed oscillator is shown in Fig. 4, which consists of two identical source degeneration amplifiers in a positive feedback configuration. The small signal loop gain is

$$Gain \approx \left(\frac{g_m Z_L}{1+g_m {Z_s}'}\right)^2, \tag{1}$$

where $Z_L = R_L \parallel C_L$, and $Z_s' = Z_s/2 + 1/(j\omega C_s)$; here $Z_s$ is the FBAR tank impedance.

At the series resonance, the source degeneration of the cross-coupled pair reaches a sharp local minimum, allowing super-unity loop gain and thus oscillation at this frequency.

In the proposed oscillator circuit (Fig. 1), we have introduced capacitors $C_L$ and $C_s$ which are of critical importance. The next section is dedicated to describing their functions.

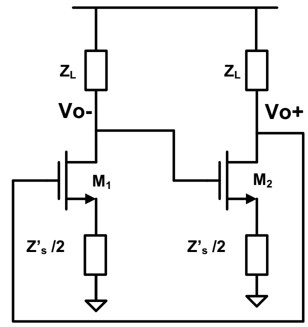


Fig. 4. The equivalent circuit of our proposed series oscillator in Fig. 1.

## III. Design considerations

### A. Prevention of parasitic oscillation

The proposed differential series FBAR oscillator in Fig. 1 has a potential parasitic oscillation at a frequency higher than the FBAR resonances $f_s$ and $f_p$. The impedance looking down into the drains of the cross-coupled pair is

$$Z = \frac{-2}{g_m}\left(1 + \frac{g_m Z_s'}{2}\right). \tag{2}$$

Eq. 2 indicates that impedance $Z$ is inductive with a capacitive source degeneration impedance $Z_s'$. $Z_L$ contains a capacitive component contributed by parasitics and explicit load capacitance. These two impedances in parallel form a parasitic resonance that can be excited at a high frequency. This can be intuitively understood by recognizing that, in addition to the series resonance frequency, the cross-coupled pair gain becomes large at high frequencies due to the drop in FBAR impedance. Fig. 5 shows a simulated result of the oscillator loop gain. In addition to the desired oscillation at the series resonance, the condition for oscillation ($|G(\omega)| >$ 0dB and $\angle G(\omega) = 0^o$) also occurs at an undesired frequency >4GHz.

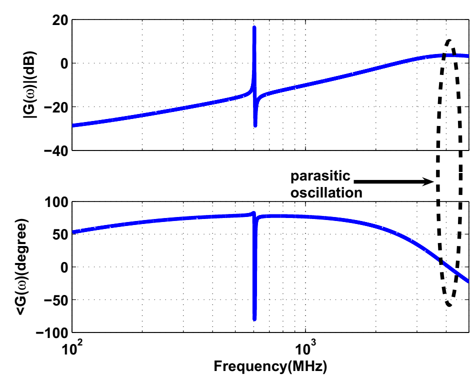


Fig. 5. Simulated loop gain showing parasitic oscillation.

Fortunately, the load impedance tank $Z_L$ provides an opportunity for low-pass filtering the loop gain transfer function to suppress the parasitic oscillation by the inclusion of an explicit $C_L$. To accommodate variations from both CMOS and FBAR processes, we have built a programmable on-chip load capacitor $C_L$ which value can be modified through a serial IO interface.

*B. Trade-off of power and phase noise performance*

For the moment, assume $C_s = \infty$. The series load impedance $R_{osc}$ experienced by the FBAR tank is the summation of the two input impedances looking into the sources of the cross-coupled pair,

$$R_{osc} \approx \frac{2}{g_m}. \quad (3)$$

We must avoid Q degradation of the FBAR tank to maximize phase noise performance. This requires that $R_{osc}$ be small compared to the tank impedance at the series resonance $R_s$, i.e.,

$$R_{osc} << R_s. \quad (4)$$

For $R_s$ typically less than 10Ω, it is extremely difficult to avoid de-Qing the FBAR tank in a series oscillator configuration. For typical FBAR resonators with impedances (defined as the impedance magnitude of $C_{plate}$ at resonance) on the order of 50Ω, a typical $R_s$ will be sub-1Ω. Even with smaller resonators, it is difficult to achieve an $R_s$ above 5 or 6Ω. Only extremely small resonators with very high impedance can achieve $R_s > 10\Omega$. This is an area of future study as it is unknown what other trade-offs there will be when going to extremely small area resonators.

We propose to address this limitation by boosting the intrinsic FBAR motional resistance to a higher value using a capacitive transformer as shown in Fig. 2(c). The simulated result of $R_s$ and $f_s$ versus $C_s$ is given in Fig. 6. Both $R_s$ and $f_s$ increase as $C_s$ decreases. With a $C_s$-tuned resonator, we

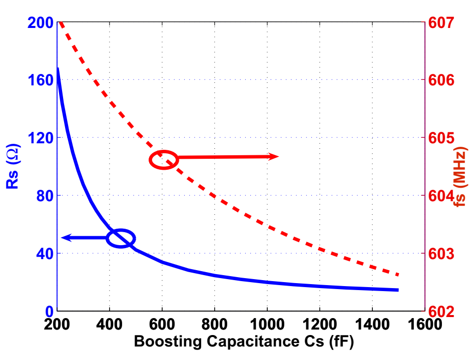


Fig. 6. $R_s$ boosting in resonant tank $Z_s'$ through a series capacitor $C_s$.

create an extra degree of freedom $C_s$ to mitigate the large current requirement resulted from the need of the minimum loaded resonator Q.

In our implementation, we design a $C_s$, so that $R_s$ of the resonator compound is approximately 50Ω. We then relax the constraint imposed by Eq. 4 so that the total loaded Q is 50% of the unloaded Q of the resonator. This requires that the nFET cross-coupled pair consume approximately 8mA current, which is about 10 times lower than without the $R_s$ boost.

A tunable $C_s$ was desired to allow for assembly of different FBAR samples. Unfortunately, since series resistance must be avoided at all costs, transistor switching was not feasible. Thus, we used multiple on-chip $C_s$ configurations that are selected through wirebonding at the packaging level. The complete oscillator schematic is shown in Fig. 7.

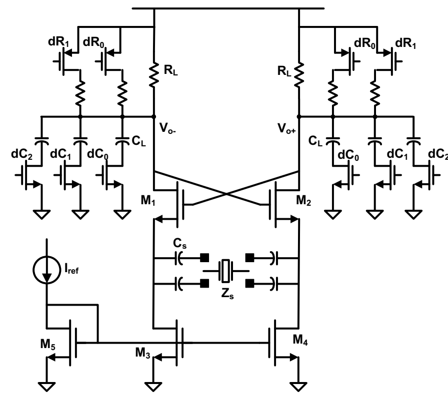


Fig. 7. Final schematic of the oscillator.

## IV. Experimental Results

The oscillator was fabricated in a 0.13$\mu$m CMOS process, occupying (500×750)$\mu$m$^2$ of area including the pads. The die photo is shown in Fig. 8. The FBAR is epoxied directly on the CMOS chip, allowing in-package assembly of the entire frequency reference.

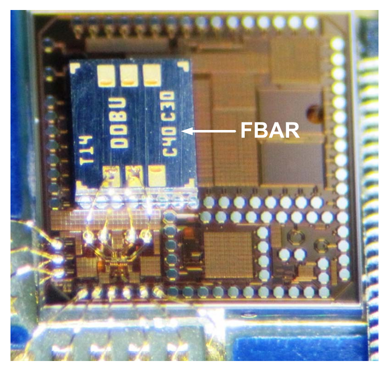


Fig. 8. Chip micrograph of the oscillator.

The oscillator operates over a supply range of 1 to 1.5V. The measured power-supply-rejection is around 730ppm/V throughout this range.

Fig. 9 shows the measured frequency spectrum of the oscillator at a supply of 1.25V. The current drawn from the supply is 4.5mA. The phase noise of Agilent PSA E4440 is typically -116 and -124dBc/Hz at 30kHz and 100kHz frequency offsets. It can be seen that the measured spectrum noise floor at offset 30kHz and above is dominated by the instrument noise. The phase noise of the oscillator measured with an Agilent 5052B (Fig. 10) is -126dBc/Hz and -150dBc/Hz at 10kHz and 1MHz offsets respectively. The integrated RMS jitter from 10kHz to 20MHz is 50fs.

Fig. 11 shows the results of the temperature sweep measurement of the oscillator. Using a compensated 600MHz FBAR

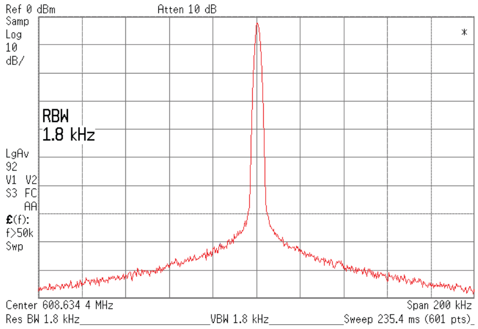


Fig. 9. The measured frequency spectrum of the oscillator with Agilent PSA E4440.

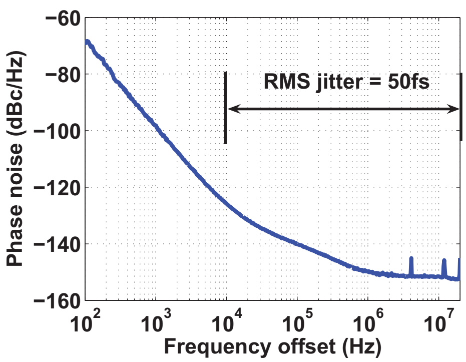


Fig. 10. The oscillator phase noise measured with Agilent SSA 5052B.

resonator, the oscillator drifts only 50ppm over a temperature range of 25 to 110$^o$C. A conventional crystal oscillator has a frequency stability in the range of ±10ppm, which includes temperature stability, aging and initial calibration.

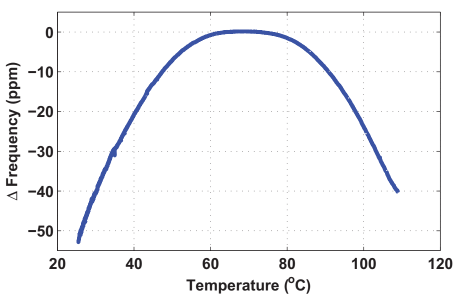


Fig. 11. Measured frequency dependence of the oscillator over temperature.

The measured frequency variation over time at a normally-fluctuating "room temperature" is shown in Fig. 12. The oscillator drifted by less than 6ppm over a 40-hour period.

Table I provides a performance summary and comparison to previously published work.

## V. Conclusion

We have presented a novel differential oscillator topology operating at the series resonance of an FBAR. The oscillator uses a cross-coupled pair with $R_s$-boosted FBAR source degeneration to realize a high Q series resonance. Our oscillator FOM is 214dB. The measured frequency stability is 50ppm over a temperature range of 25 to 100$^o$C. This oscillator provides the potential to replace quartz oscillators in applications where size and cost are critical.

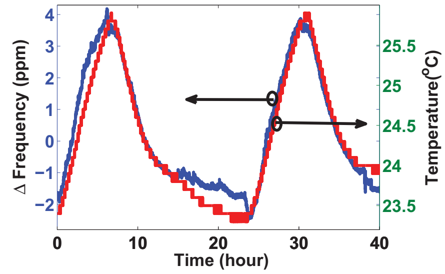


Fig. 12. Frequency stability at room temperature.

Table I
Performance Summary

| | this work | [7] | [2] | [4] |
|---|---|---|---|---|
| CMOS process | 0.13$\mu$m | 0.5$\mu$m | 0.18$\mu$m | 0.35$\mu$m |
| $f_c$ (MHz) | 600 | 223 | 1917 | 600 |
| $V_{dd}$ (V) | 1.25 | 5 | 1 | 3.3 |
| Power (mW) | 5.6 | 10 | 0.3 | 17.5 |
| £(f)@100Hz (dBc/Hz) | -69 | -60 | – | – |
| £(f)@1kHz (dBc/Hz) | -98 | -88 | – | -102 |
| £(f)@10kHz (dBc/Hz) | -126 | -121 | -100 | -130 |
| £(f)@100kHz (dBc/Hz) | -140 | -148 | -120 | -149 |
| £(f)@1MHz (dBc/Hz) | -150 | -160 | -130 | – |
| Int. RMS jitter (10k-20MHz) (fs) | 50 | – | – | – |
| Temperature drift (ppm) | ~50 (25−110$^o$C) | – | 2125 (25−110$^o$C) | 80 (-35−85$^o$C) |
| FOM(dB) | 214 | 205 | 211 | 213 |

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