A 3 μW, 400 MHz Divide-by-5 Injection-Locked Frequency Divider with 56% Lock Range in 90nm CMOS

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Abstract — **An ultra-low power injection locked frequency divider (ILFD) is presented and demonstrated. Based on a 5-stage single ended ring oscillator, the ILFD achieves a lock range of 56% at a division ratio of 5 in the medical implant communications service (MICS) and the 433MHz ISM frequency bands. The ILFD is implemented in a 90nm CMOS process. It consumes 3 μW of power from a 1.0V supply and 100 μm^2 of area. The circuit achieves a frequency divider figure-of-merit of 134 GHz/mW.**

Index Terms — **frequency division, injection locking, ring oscillator, injection locked frequency divider, ILFD, low power design, MICS**

I. Introduction

The emerging need for implantable and body-worn medical diagnostic devices demands miniaturized form-factors and extremely low power consumption wireless links operating in the 402-405 MHz MICS band and the 433 MHz ISM band [1]. Typically, the frequency synthesizer (Figure 1) in a wireless transceiver consumes a large portion of the power and die area, and within the synthesizer, the VCO and the frequency divider are the dominant contributors. Significant effort has been made in reducing the die area and power consumption of VCOs [2]. Introducing a low power divider as a pre-scaler relieves the subsequent digital dividers from operating at the full RF frequency, reducing the total synthesizer power consumption.

Injection-locked frequency dividers (ILFDs) are based on the principle of locking a low frequency oscillator to an incoming signal at its Mth harmonic [3] – [5]. Since they operate at a frequency M times lower than the VCO, ILFDs consume significantly less power than traditional digital implementations. Recently, a number of ILFDs have been reported based on either on-chip LC oscillators or ring oscillators. On-chip LC tanks generally consume a large silicon area, which render the LC oscillator-based ILFD an inferior solution in the sub-GHz MICS and ISM bands. Ring oscillators, on the other hand, are extremely small in area. In addition, they generally have a larger locking range because of their lower Q. Although the phase noise of traditional ring oscillators is high, the noise performance improves dramatically when locked to a clean reference.

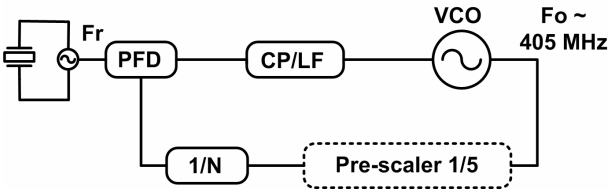

Figure 1. Architecture of ultra-low power MICS band frequency synthesizer

A few recent publications focus on designing ring oscillator-based ILFDs. References [6]—[9] consume more power than acceptable in energy constrained applications such as implanted MICS transceivers. Reference [10] demonstrates low power consumption, but the division ratio of 2 limits the effectiveness of the pre-scaler in reducing digital divider power consumption.

This paper introduces a new ring-oscillator based ILFD architecture fabricated in 90 nm CMOS. This ILFD consumes 3 μW and can achieve 56% lock range at a division ratio of 5 with an input frequency of 405 MHz. Section II introduces the architecture. Section III discusses the design and implementation issues. Section IV presents the experimental results, followed by some conclusions.

II. The Proposed ILFD

We have chosen an injection locked ring oscillator topology for this MICS/ISM band frequency divider. In a typical 90nm CMOS process, an 80 MHz ring oscillator can operate with approximately 1μW from a 1V supply, affording extremely low power operation.

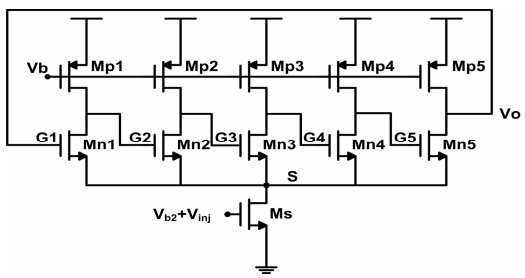

Figure 2. Proposed ILFD based on a 5-stage ring oscillator

The proposed ILFD is displayed in Figure 2, where the injection points are simultaneously applied with an RF frequency V_{inj} to each of the 5 stages of a modified ring oscillator. The same topology is extendable to n stages to accomplish a division ratio of n, where n is an odd number equal to or larger than 3.

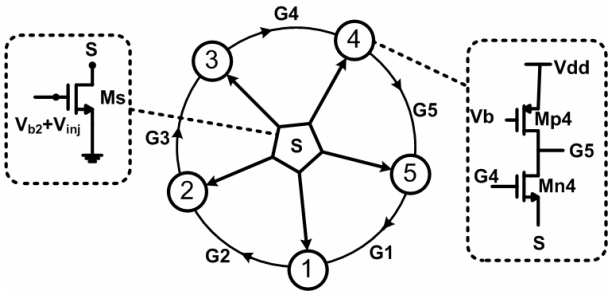

Figure 3. Conceptual drawing of the sequential injection at the 5th harmonic of the oscillator

It can be shown that a free running oscillation can be pulled or tuned to a different oscillation frequency when it is impressed with an external oscillatory force at a nearby frequency [3] – [5]. Our design applies such a force at the tail by injecting a periodic current at a frequency 5 times that of the free running ring. This is more intuitively illustrated by Figure 3, where an external signal is applied to the common point so that each of the 5 stages draws current sequentially.

It is assumed that each stage of the ILFD, when locked, can be modeled as a non-linear block and a linear block as shown in Figure 4.

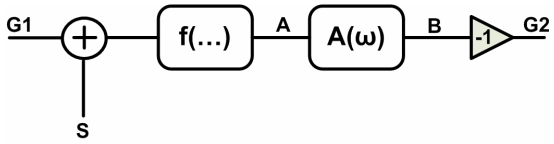

Figure 4. Analytical model for one stage of the ILFD

Function f(…) describes a non-linear transformation on the summation of two signals: the input voltage to the gate and the corresponding injection input at source node S. The signal at node S represents the injected RF signal into the stage. During oscillation, the voltages at G1, G3, G5, G2, and G4 have large swings and are evenly phased with G1 leading G3, G3 leading G5 and so on. Since all sources of the ring oscillator are shared, the common node experiences a large 5th harmonic component. Thus, when the ILFD is in the locked condition, with an injection frequency of $5\omega_o$ applied to V_{inj}, where ω_o is the ILFD output frequency, the actual strength of the injected current that reaches the individual stage has strong 1st to 5th harmonics of ω_o. When locked, the non-linear block combines this input together with a strong tone of ω_o as well as its harmonics at G1 and generates a strong frequency component of ω_o at node A.

The linear block $A(\omega)$ in Figure 4 models the phase shift and the gain of the signal from G1 to G2 for small signals. Typically, it appears as a first order low pass response, i.e.

$$A(\omega) = A_0 /(1 + j\omega/\omega_p) \qquad (1)$$

where A_0 is the low frequency gain and ω_p is a pole contributed by the (parasitic) load capacitor at G2. ω_p is directly related to the free running frequency of the oscillator. Higher frequency terms resulting from the nonlinear block are filtered by the linear block with a cut-off frequency close to the output frequency ω_o. DC and lower frequency terms are rejected by the oscillation loop which has a total DC phase offset of π. In order to maintain a successful frequency lock, the signal needs to have a total gain of 1 and phase shift of $2\pi/5$ from G1 to G2.

Since a higher Q oscillator tank results in a sharper band-pass characteristic, for the same topology the frequency lock range decreases as the number of stages is increased in a ring based ILFD. This implies that the lock range is reduced when the same topology is used for higher division ratios. To satisfy the Barkhausen criterion for oscillation, the injection signal must be strong enough to provide the additional gain needed. The further the lock frequency is away from the free running frequency, the stronger the injection signal needs to be. Additionally, when the bias current in the stage is increased, DC gain A_0 is relatively unchanged and pole frequency ω_p is increased, as the output impedance of each stage is reduced. Thus, consuming more power makes the lock frequency higher and the absolute lock range wider, but has little influence on the relative locking range.

III. Circuit Implementation

The circuit was implemented in a 90 nm CMOS process and occupies 100 μm^2 of silicon area (refer to highlighted area in Figure 5). It operates from a 1.0V power supply. A few circuit design considerations are provided in this section.

Although the ILFD is similar to a standard digital ring oscillator, the device sizes and operating points must be carefully chosen to ensure high injection efficiency. For example, linear gain block $A(\omega)$ is determined by the inverter output conductance (Figure 2) and the parasitic load capacitance. The injection transistor Ms supplies

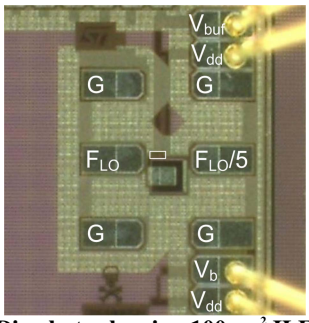

Figure 5. Die photo showing 100μm² ILFD and GSG RF input/output

bias current to the ring oscillator and provides an RF transconductance (g_m) converting the RF input signal into a perturbation current injected into the oscillator.

Since the operating frequency of the ILFD is determined by the starved current through each stage and the capacitive loading, there is a significant power benefit for moving to smaller processes with higher f_T. However, process variation will cause stage-to-stage delay mismatch, which becomes more severe at advanced technology nodes. Large transistor sizing mitigates this mismatch at the penalty of increased power dissipation and reduced free-running frequency. The layout of the five divider stages must be extremely well matched to ensure equal phase delay through each stage - imbalanced stages will result in a decreased frequency lock range. For the divider to drive a large load (either instrumentation or subsequent digital dividers in a synthesizer), the output buffer needs to be sized up gradually so that it imposes a small load to the ring. Alternately, a larger buffer with replica loading on each stage can be used at the expense of power consumption.

IV. Experimental Results

Figure 6 illustrates our test setup. An Agilent E4438C ESG and an Agilent E4446A PSA are used for RF frequency generation and output spectrum analysis, respectively. Figure 7 is the "V-curve" demonstrating the ILFD lock range. Below an RF input power of -22 dBm, the oscillator loses lock and runs free. As the injection power increases, the frequency lock range increases, so does the oscillator free running frequency. A higher free running frequency is reflected by the higher center frequency of the lock range. With an input power of -10 dBm, the input-referred lock range is approximately 371 to 664 MHz, providing a relative frequency lock range of 56%.

Figure 8 shows the locked and unlocked spectra overlaid for comparison. As expected, the signal tone is

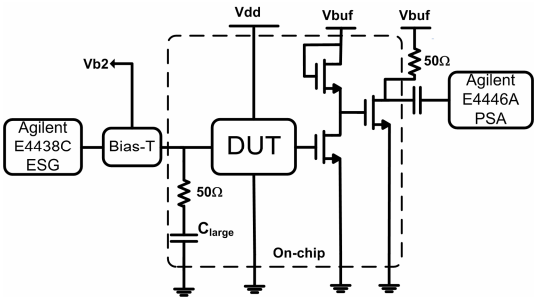

Figure 6. Experimental test setup. GSG wafer probes applied at the RF input

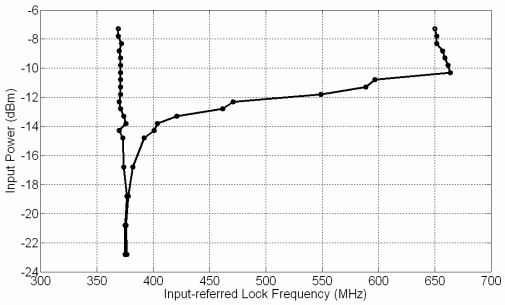

Figure 7. Frequency lock range of the ILFD

much sharper and noise floor is significantly lower when the oscillator is in a locked state. Figure 9 shows the measured phase noise performance at the divider's output in a locked state compared with free-running mode. The signal source phase noise assuming an ideal divide-by-five is plotted for comparison. The divider power consumption scales linearly with operating frequency. Over the 371-664 MHz lock range, the divider power consumption scales from 2.67 to 5.07 μW (measured with an RF power of -8.5 dBm). Table 1 presents a comparison of this work with previously published ring oscillator based ILFDs. This work achieves the highest figure-of-merit (defined as the input referred-frequency normalized to the divider DC power consumption) reported to date: 134 GHz/mW.

V. Conclusions

A new ring oscillator based ILFD is proposed and experimental results presented. A detailed performance summary is given in Table 2. This divider consumes 3μW at 400 MHz and is suitable for use in ultra-low power transceivers operating in the 405 MHz MICS and 433 MHz ISM bands. This work achieves the highest injection locked frequency divider figure-of-merit reported to date.

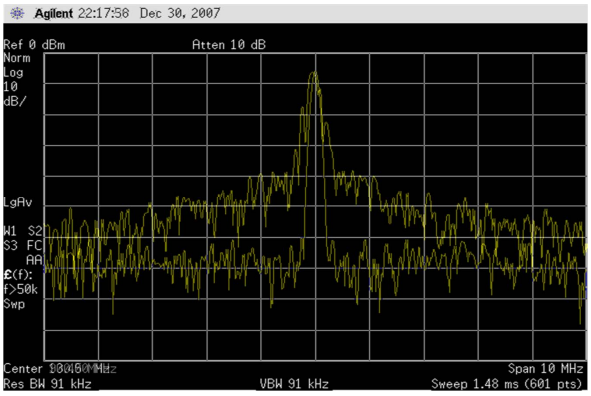

Figure 8. Free-running and locked spectra overlaid for comparison for an RF input of 500MHz

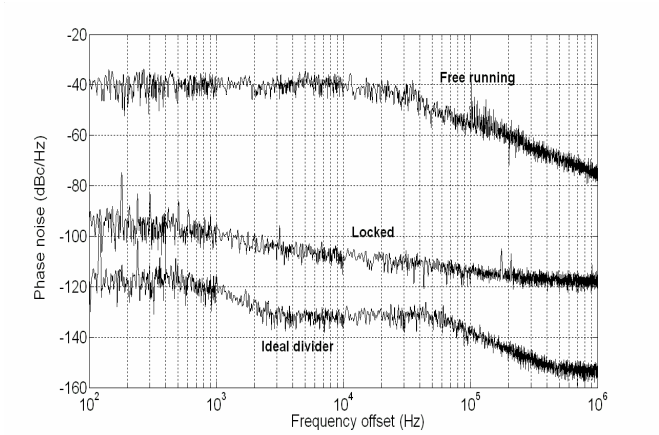

Figure 9. Phase noise performance of the ILFD compared with that of free running oscillation and the RF signal source alone

TABLE 1.
PERFORMANCE COMPARISON WITH EXISTING WORK

	Process (CMOS)	Power (mW)	Input Power (dBm)	Div. Ratio	Lock Range (GHz)	Lock Range (%)
This work	90 nm	0.003	-10	5	0.37-0.66	56
[6]	0.18μm	3.6	3	8	9.2 – 12.3	30
[7]	0.18μm	7.2	-10	6	1.9 – 4.0	71
			3	12	5.7 – 7.6	29
			3	18	9.5 – 11.2	16
[8]	0.18μm	9.8	0	2	1.9 – 3.65	63
		17.64	0	2	2.95 – 5.5	60
[10]	0.20 μm	0.044	0	2	2.0 – 4.3	73
[9]	0.13μm	10.4	2	2	4 – 6	40
		10.4	5	4	9 –11	20
		12.5	11	6	14.5 –15.3	5
		12.5	13	8	20 – 20.15	0.8

TABLE 2. DESIGN AND PERFORMANCE SUMMARY

Technology	90 nm CMOS @1.0V
Silicon area	100 μm^2
Lock range	371-664 MHz (56%)
Power consumption	< 3 μW @ 400 MHz
Input power at max. lock range	-10 dBm
Phase noise	-120dBc/Hz @1MHz

VI. ACKNOWLEDGEMENTS

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VII. REFERENCES

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