A 750μW 1.575GHz Temperature-Stable FBAR-Based PLL

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***Abstract*—A 1.575GHz phase-locked loop (PLL) using a bulk acoustic wave resonator (FBAR) based VCO is presented. Close-in phase noise is suppressed by the loop, while high-offset noise is suppressed by the extremely high Q (>2000) VCO. This technique results in a 750μW PLL with phase noise of -82 and -138dBc/Hz at 1kHz and 1MHz offset, respectively. A temperature-compensated FBAR stack is described, allowing quartz locking over a -10 to 100 °C temperature range.**

I. Introduction

High performance portable wireless applications, GPS receivers [1] and high speed ADCs increasingly demand the generation of GHz frequency references with low phase noise (jitter), high stability, and low power consumption. Additionally, reference generation at frequencies higher than quartz can provide is increasingly needed for very wide bandwidth or high frequency PLLs [2]. Traditional frequency synthesizers with on-chip LC resonators achieve low phase noise by running high VCO bias current and utilizing a wide PLL loop bandwidth [3]. When LC resonators are replaced by miniaturized bulk acoustic wave (BAW or FBAR) resonators, superior phase noise and power performance can be simultaneously achieved [4][5][6]. These miniaturized resonators are fabricated in CMOS-compatible silicon processes, allowing low unit cost and promising eventual integration with CMOS. However, uncompensated FBAR resonators have a temperature coefficient of approximately -28ppm/ °C [7], making it difficult for the PLL to cover a wide temperature variations given the limited tuning range of FBAR oscillators. In this paper, we introduce a PLL architecture with a temperature compensated FBAR resonator that allows locking to a stable reference from -10 to 100 °C.

We present the first PLL that employs an FBAR resonator, allowing a VCO quality factor approximately two orders of magnitude higher than traditional PLLs. The PLL output frequency inherits the accuracy and close-in purity of the reference while providing a 30 dB improvement in phase noise at high-frequency offsets compared to traditional VCOs for a given power consumption. The PLL runs at 1.575GHz and has a tuning range of 1.3MHz. The entire PLL dissipates 750μW from a 1V supply and demonstrates 0.6ps of integrated RMS jitter from 10kHz to 10MHz and phase noise of -82dBc/Hz and -138dBc/Hz at 1kHz and 1MHz offsets, respectively. With a temperature-compensated FBAR, the PLL is able to lock to the reference frequency over a 110 °C temperature range. Measured results from an identical PLL using an on-chip 10nH inductor (Q=8) instead of the FBAR is presented for comparison.

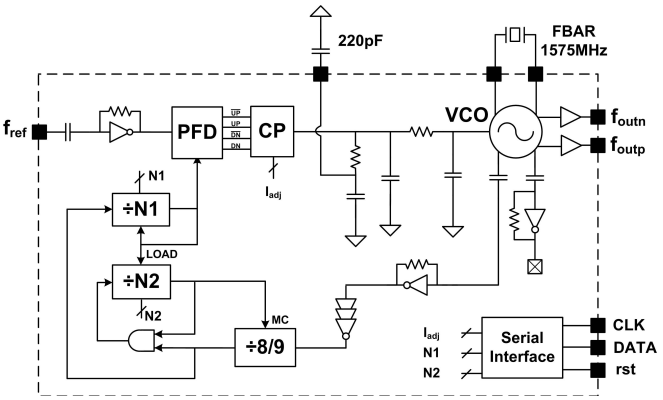

Fig. 1. The integer-N FBAR-based PLL architecture.

II. Proposed Architecture

Figure 1 shows the proposed integer-N type-II PLL architecture. Figure 2 is a plot of Q vs. frequency of an uncapped FBAR resonator from a modified Butterworth-Van-Dyke (mBVD) model. The resonator presents a maximum Q value near the parallel resonance. The rapid roll-off of the FBAR Q as a function of frequency fundamentally limits the VCO tuning range. The low phase noise of the FBAR VCO allows the PLL to operate at a low loop bandwidth for an optimal overall PLL phase noise performance. The low VCO gain derived from the high Q resonator helps to maintain a small loop bandwidth without excessively reducing the charge pump current. This, in turn, leads to a low noise contribution from the charge pump and the loop filter.

The combination of very low VCO gain and low loop bandwidth significantly reduces the magnitude of the reference spurs originating from mismatch in the phase frequency detector (PFD) and the charge pump. In our proposed architecture, a 3^{rd} order loop filter is deployed to further reduce the reference spurs. An integer-N architecture was used to avoid fractional spurs for applications that demand a very clean RF reference.

The frequency divider uses an 8/9 dual-modulus prescaler programmable through two 4-bit adjustable counters N1 and N2. The low power of the VCO demands careful design in the prescaler to reduce its relative power contribution. The prescaler is implemented with true signal-phase-clock

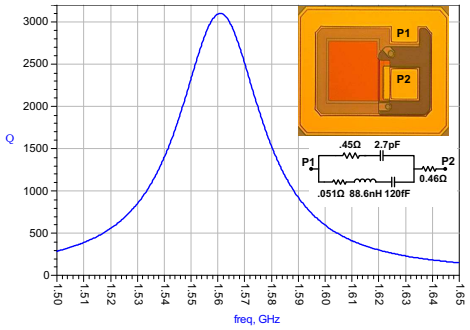

Fig. 2. Q vs. Frequency of an uncapped FBAR resonator.

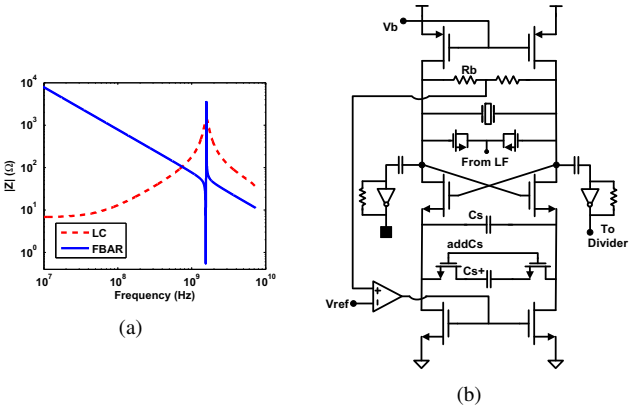

Fig. 3. (a) Tank impedance of FBAR and LC resonators. (b) The schematic of the VCO.

(TSPC) dynamic logic in order to obtain a better power-delay efficiency over static CMOS implementations.

To make a performance comparison with an LC-based PLL, the same PLL architecture is duplicated on the same die with the FBAR resonator replaced by an on-chip inductor. The two VCOs differ drastically in tuning sensitivity. As a result, their VCO gains differ significantly. Both PLLs achieve similar phase margin using the same loop filter through a programmable DAC for charge pump current.

Programmability of the charge pump current and the divider ratio are realized through the built-in serial data interface. The loop filter uses one 220pF off-chip capacitor. The FBAR PLL configuration exhibits a loop bandwidth of 10kHz with a phase margin of approximately 65 ° (60kHz with a 55 ° phase margin for the LC PLL).

III. Circuit Description

A. The Voltage-Controlled Oscillator

Unlike an LC-tank, the FBAR presents a high capacitive impedance at low frequencies. Figure 3(a) shows an impedance magnitude comparison of an LC vs. an FBAR tank. Thus, the VCO uses a common-mode feedback (CMFB) loop and a high-pass negative resistance response provided by capacitive source coupling to ensure low-frequency stability (Figure 3(b)). A larger Cs value reduces the oscillator stability as the high-pass cut-off frequency gets lower. On the other hand, a smaller Cs reduces the transconductance of the cross-coupled pair, hence requiring more power to achieve oscillation. Cs is programmable to accommodate a variety of resonator impedances.

VCO tuning is provided by two small (6μm$\times 6\mu$m) NMOS varactors shunting the resonator tank; excessive capacitive loading degrades the already-limited tuning range of the VCO. The cross-coupled transistors present a significant capacitive load to the tank. Reducing their size improves tuning range at the cost of increased power consumption.

Resistive loading reduces the Q of the resonant tank, ultimately degrading the phase noise performance of the PLL. With a typical impedance value over 3kΩ at the parallel resonant frequency, resistive loading on the FBAR tank should be above 30kΩ to reduce resonator Q degradation. The four-stage divider buffer was designed to minimize resistive and capacitive loading to the VCO, which would degrade the oscillator Q and tuning range, respectively.

B. The Phase Frequency Detector

The schematic of the phase frequency detector (PFD) is shown in Figure 4. One of the design considerations is to minimize the reset path delay. A short reset path can lead to the dead zone problem and a long reset path can cause large reference spurs. By combining a fast responding charge pump, the achievable minimum delay reset path is sufficient to avoid a dead zone problem.

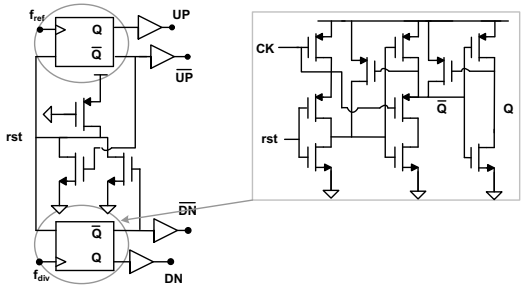

Fig. 4. Schematic of the phase frequency detector.

The D flip-flops are implemented using dynamic logic. The two weak pull-up PMOS ensure a low frequency operation by replenishing charge leaking through the NMOS when the logic is **1**. This dynamic implementation has been shown to provide a faster reset path over static logic implementations. The reset feedback path uses a single stage logic, with a weak constantly-on PMOS to minimize the logic **1** output path.

C. The Charge Pump

The charge pump (CP) is biased with a 5-bit current DAC and an on-chip current reference (Figure 5). The DAC provides programmability of the charge/discharge current, a requirement for loop stability control since the two PLLs (FBAR and LC) have vastly different VCO gains. To support a wide output voltage swing (and thus tuning range), the charge pump employs OTA1 to enhance up- and down-current

matching. OTA2 reduces the effect of charge injection to help suppress reference spurs. Both OTAs use a folded cascode topology and consume 12μA while providing a voltage gain greater than 40dB.

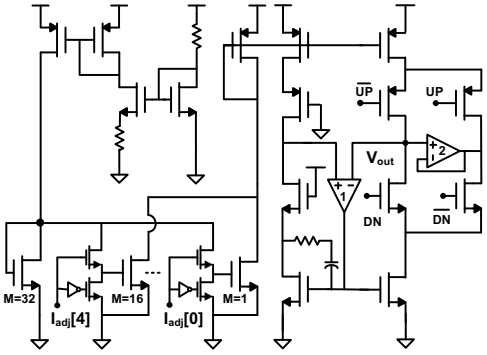

Fig. 5. Schematic of the charge pump.

IV. Mechanical Temperature Compensation of FBARs

A mechanically temperature compensated FBAR resonator was utilized, providing <150ppm temperature stability over the -10-100 °C temperature range (compared to approximately 3080ppm for an uncompensated resonator). This modified FBAR consists of a free standing membrane approximately 2μm in total thickness and approximately 45,000μm^2 in area. The unloaded Q of these resonators at the anti-resonance (parallel) mode is 3000. To achieve this temperature stability, a thin oxide layer with a positive temperature coefficient (TC) is added to the acoustic stack [7]. This offsets the negative temperature coefficient of the piezoelectric aluminum nitride (AlN) and the molybdenum (Mo) electrodes. By adding this thin layer, we cancel out the linear frequency dependence on temperature and are left with the quadratic term (β is approximately -28ppb/°C^2).

V. Experimental results

The design was fabricated in a 0.13μm CMOS process, occupying 320μm×250μm for the FBAR PLL and 320μm×550μm for the LC PLL, both excluding pads. The 560μm×705μm FBAR die is wire-bonded directly to the 0.13μm CMOS die (Figure 6), allowing placement in a single IC package. Alternatively, the FBAR die can be flip-chip bonded onto the CMOS at the wafer or die level. The chip operates at a supply voltage of 1.0V and a total power dissipation of 750μW (500μW for the VCO and 250μW for the rest of the circuitry, including divider, divider buffer, CP, PFD, and crystal buffer). The LC VCO exhibits a gain (Hz/V) over 80 times larger than the FBAR VCO. The measured VCO tuning curves are shown in Figure 7. The measured settling time of the FBAR PLL is 600μs with a CP current of 10μA (Figure 8). Measured results are consistent across all divide ratios (30-130).

Figure 9 shows the phase noise of the locked and free-running FBAR VCO measured with an Agilent E5052B signal source analyzer. An external 45MHz crystal oscillator was used as the reference with a divide ratio N=35 (f_c=1575 MHz). The measured crystal reference phase noise, scaled by 20·log(N) dB, is plotted to illustrate the reference noise contribution. Additionally, the phase noise of the locked LC PLL is shown for comparison. The measured phase noise of the FBAR PLL is -138dBc/Hz at 1MHz offset, 37dB lower than the LC PLL operating at the same VCO power consumption. Close-in phase noise of the FBAR PLL is dominated by the reference phase noise contribution: -75dBc/Hz at 100Hz offset, which is nearly 20dB better than that of the LC PLL. Figure 10 presents measured frequency spectra of the FBAR and LC PLLs in locked state overlaid for comparison. PLL noise shaping of the LC spectrum up to the loop bandwidth of 60kHz is clearly visible, while the close-in noise of the FBAR VCO is instrument-dominated. The measured reference spur level of the FBAR PLL is -77dBc, 11dB lower than the LC version due to a lower loop bandwidth and a higher charge pump current. The integrated RMS jitter from 10kHz to 10MHz is 0.6ps for the FBAR PLL and 20ps for the LC PLL.

The measured temperature stability of the FBAR VCO in both free-running and locked states is shown in Figure 11. Mechanical temperature compensation of the resonator allows locking to a fixed reference over a wide temperature range even with a limited VCO turning range. Table I provides a performance summary of the FBAR and LC PLLs.

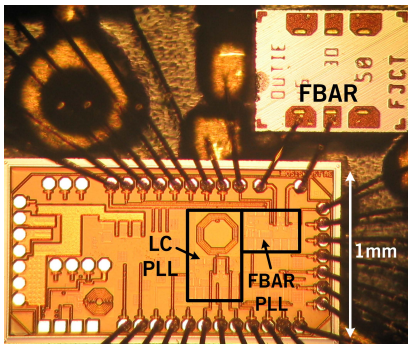

Fig. 6. Chip micrograph of the FBAR and LC PLLs.

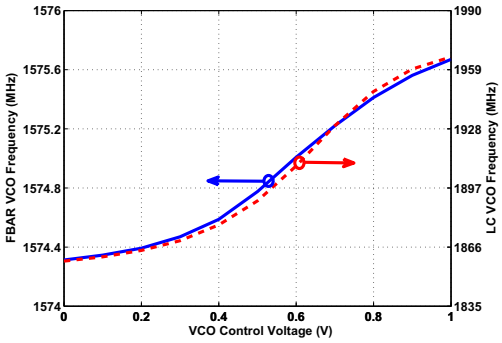

Fig. 7. Measured FBAR and LC VCO tuning range.

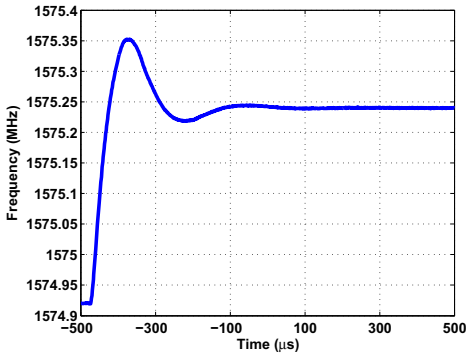

Fig. 8. PLL settling time measurement using an Agilent 5052B signal source analyzer.

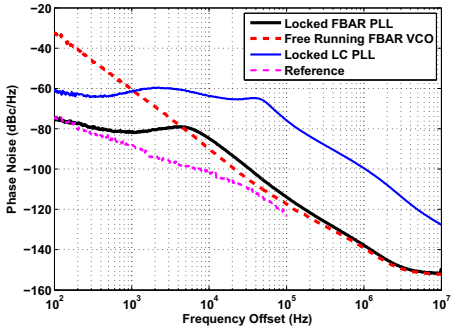

Fig. 9. Measured phase noise performance comparison.

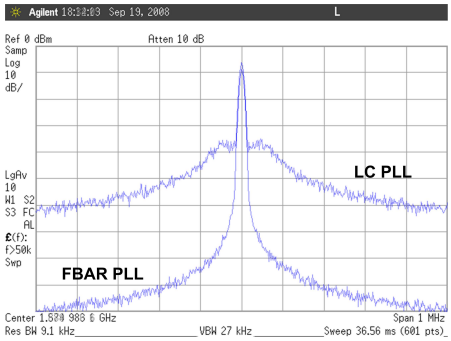

Fig. 10. Measured close-in frequency spectra of locked FBAR and LC PLLs.

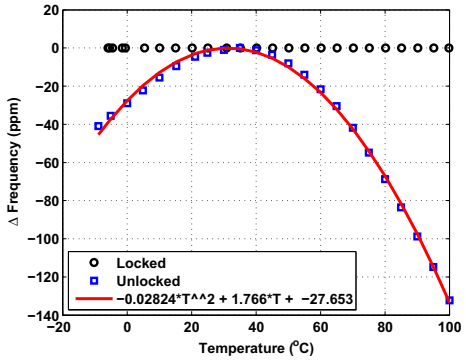

Fig. 11. Frequency vs. temperature stability measurements.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

		FBAR PLL	LC PLL	[8]
Process (CMOS)		0.13μm		0.13μm
V_{DD}(V)		1.0		1.2
PLL type		type-II int-N		type-II int-N
f_{center} (GHz)		1.575	1.89	2.0
f_{ref} (MHz)		45	45	250
Loop BW(kHz)		~10	~60	~10,000
Tuning range(MHz)		1.35	107	2,000
Power (μW)	VCO	500	500	9,000
	Divider	~95	~115	-
	PFD/CP/XTL Buf	~60	~40	-
	Divider Buf	~95	~115	-
	Total	750	770	23,000
Reference spur (dBc)		-77	-66	-68.5 to -48
Phase noise (dBc/Hz)	At 1kHz	-82	-61	-82
	At 10kHz	-85	-62	-106
	At 100kHz	-114	-75	-118
	At 1MHz	-138	-101	-125
	At 3MHz	-149	-113	-120
Integrated RMS jitter (ps)	1kHz-40MHz	1.4	24.8	0.58
	10kHz-10MHz	0.6	20	-

VI. Conclusion

This paper presents a 750μW 1.575GHz FBAR PLL enjoying the phase noise/jitter benefits of a Q>2000 VCO tank while inheriting the stability and in-band phase noise suppression of a low frequency reference. This architecture provides a low power, low jitter, high frequency reference for local oscillators, sampling clocks, and wide-bandwidth PLLs.

Acknowledgment

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