A Wide-Tuning Digitally Controlled FBAR-Based Oscillator for Frequency Synthesis

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***Abstract*—This paper presents a wide-tuning digitally controlled FBAR-based oscillator in a 0.18μm CMOS process. The oscillator is tuned with a digitally-switched capacitor array to achieve a tuning range of >7000ppm, an over eight-fold improvement over previously published low power FBAR-based VCOs. The high Q FBAR allows frequency tuning to be implemented with a switched-capacitor array with relatively large unit capacitors to achieve a sufficiently fine resolution for frequency synthesis. Our oscillator achieves a measured phase noise of -99dBc/Hz and -142dBc/Hz at 10kHz and 1MHz offsets respectively at a carrier frequency of 1.50GHz while consuming less than 4mW.**

I. Introduction

After more than a decade of technical improvement and application development, thin film bulk acoustic-wave resonator (FBAR) technology has matured to fill a variety of applications that require miniaturization and low cost in high-Q duplexers, multiplexers, and filters used in mobile communication systems and other wireless applications [1][2]. In the meantime, a significant amount of work has been performed on using FBAR resonators in low power oscillators and frequency synthesizers [3][4][5]. One significant drawback of FBAR-based oscillators is the limited tuning range, which is typically less than 1000ppm. In this paper, we demonstrate a circuit toplogy that allows a low power, low phase noise FBAR oscillator with a tuning range >7000ppm. The resulting digitally-controlled oscillator (DCO) has several potential applications, including frequency references and frequency synthesis (Fig. 1). Currently, on-chip LCs oscillators are the preferred technology for integrated frequency generation. However, on-chip LC-based VCOs consume a significant portion of the power budget in many wireless transceiver chips. The limited Q of inductors available in standard IC processes (typically less than 20) limits further performance improvement of RF frequency synthesizers. The high Q characteristic of the FBAR (greater than 2000) lends itself to applications that demand low phase noise, low jitter, and low power. Previous works have demonstrated that FBAR-based oscillators and synthesizers can have excellent phase-noise performance at an extremely low power [3][4][5]. To be a viable RF frequency reference for high data rate applications, FBAR-based oscillators must exhibit a reasonable tuning range.

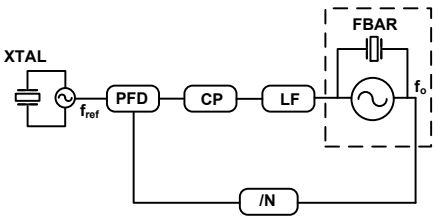

Fig. 1. Emerging applications of FBAR frequency synthesizers require sufficient tuning range to cover process variations, spread spectrum modulation, and multi-channel tunability.

An uncompensated FBAR has a temperature coefficient of about -25ppm/^{o}C [6]. In recent years, physical temperature compensation has been demonstrated to cancel, to first order, the the FBAR temperature coefficient. A zero-drift resonator (ZDR) can have an average temperature dependence of 1ppm/^{o}C over 100^{o}C temperature variation [6]. This creates promising opportunities for FBAR-based oscillators. Besides fixed frequency applications, e.g., RF frequency references for high speed ADCs and high frequency PLLs (mm-wave PLLs) (Fig. 1), a wider tuning range of an FBAR-based VCO allows moderate frequency modulation. For example, in the serial ATA application, an oscillator must have more than 5000ppm tuning capability to provide a spread-spectrum reference that is EMI compliant (Fig. 2) [7][8]. Earlier works [5] [4] [9] show a tuning range of under 1000ppm. The objective of this work was to demonstrate an FBAR-based VCO with a tuning range >7000ppm without compromising the power and phase-noise performance of the oscillator.

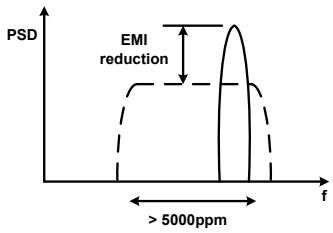

Fig. 2. In Spread-spectrum applications, such as in serial ATA, at least 5000ppm frequency tuning is needed.

Section II describes the FBAR and its capacitive tuning characteristics. Section III elaborates on wide-band FBAR-based oscillators. Experimental results and conclusions are presented in Sections IV and V.

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II. FBAR and its Capacitive Tuning Characteristics

The FBAR is a micro-electro-mechanical resonator fabricated in a planar silicon process. It exhibits a series resonance f_s and parallel parallel resonance f_p. A typical FBAR tank impedance plot is shown in Fig. 3. The resonances are determined by the thickness and mechanical properties of the piezo-electric film and metal electrodes. The FBAR structure can be described by the modified Butterworth Van Dyke (mBVD) model (Fig. 4). This model approximates the electrical behavior of the FBAR near its resonances. The R_m, L_m, and C_m describe the motional resonance caused by the piezoelectric effect of the film. R_o and C_o are the parasitic capacitance and resistance of piezoelectric film and the electrode plates. R_{ser} represents the resistance of the electrodes P_1 and P_2.

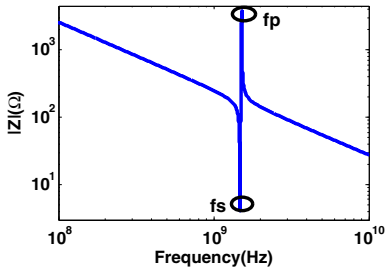

Fig. 3. Magnitude of tank impedance vs. frequency of an FBAR. The FBAR presents a high Q series resonance f_s and parallel resonance f_p.

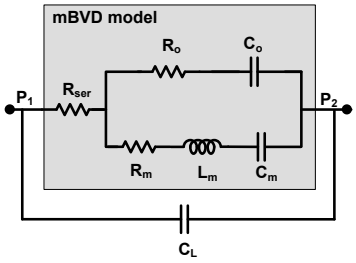

Fig. 4. The mBVD model for the FBAR with a capacitive load. Compared to an on-chip LC tank, the resonant frequency is much less sensitive to capacitive loading, while the impedance at resonance is much more sensitive.

The Q value peaks between the two resonant frequencies f_s and f_p at over 2,000, which is about 100x higher than that of an on-chip LC tank. The coupling between the electrical and mechanical domains is described by the coupling coefficient

$$K_t^2 = \frac{\pi^2(f_p - f_s)}{4f_s}$$

which quantifies the frequency difference between the two resonances. A typical value of K_t^2 is between 3% and 7% for aluminum nitride FBARs [10]. K_t^2 fundamentally determines the tuning range of the FBAR VCO.

Frequency tuning of a VCO is usually performed by a shunt capacitive tuning device (Fig. 4). Let us assume the total capacitive load to the resonator tank is C_L. The frequency tuning sensitivity is

$$\frac{\delta f_p}{\delta C_L} = -\frac{f_s}{2}\frac{1}{\sqrt{1+\frac{C_m}{C_o+C_L}}}\frac{C_m}{(C_o+C_L)^2}. \quad (1)$$

With a typical FBAR, $C_o/C_m > 20$, hence,

$$\frac{\delta f_p}{\delta C_L} \approx -\frac{f_s}{2}\frac{C_m}{C_o+C_L}\frac{1}{C_o+C_L}. \quad (2)$$

In comparison, for an on-chip LC-tank tuned similarly with a C_L, the frequency tuning sensitivity is

$$\frac{\delta f_p}{\delta C_L} = -\frac{f_p}{2}\frac{1}{C_o+C_L}, \quad (3)$$

where C_o is the parallel resonant capacitor of the LC tank. This suggests that the f_p of an FBAR is over 100x less sensitive to capacitive tuning than an LC tank. In addition, Equation 2 indicates that the frequency tuning sensitivity of an FBAR falls quadratically with C_L. In contrast, the frequency tuning sensitivity of the on-chip LC tank changes relatively slow as C_L increases. This fact conspires to further degrade the tuning range of FBAR oscillators.

In general, using a capacitive load to tune an LC tank comprising a lossy inductor reduces its tank impedance at the resonance R_p. The tuning sensitivity is

$$\frac{\delta R_p}{\delta C_L} = -\frac{L}{R_s(C_o+C_L)^2} = -\frac{Q}{2\pi f(C_o+C_L)^2} \quad (4)$$

R_p reduction is highly undesirable, as reduced R_p value demands higher power consumption for the oscillator to sustain oscillation.

Fig. 5 shows a calculation of the f_p and R_p of an FBAR tank as a function of the loading capacitance C_L.

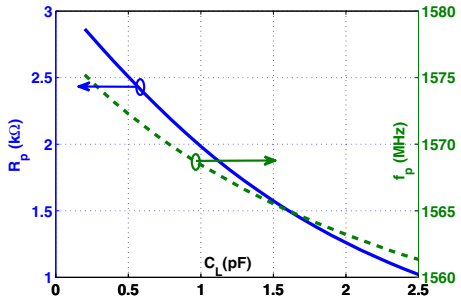

Fig. 5. Calculated R_p and f_p as a function of C_L. Initial load C_L must be minimized to achieve a wide tuning range, as f_p reduces faster at lower C_L and rapid R_p reduction sets a upper limit on C_L.

The FBAR tuning characteristics suggest that we need to carefully design the oscillator so that the initial capacitive load to the FBAR tank is minimized.

III. The Proposed FBAR-Based Oscillator

The high sensitivity of the FBAR's tuning range to the initial capacitive loading requires a close examination on the design strategy of the FBAR oscillator. In particular, in order

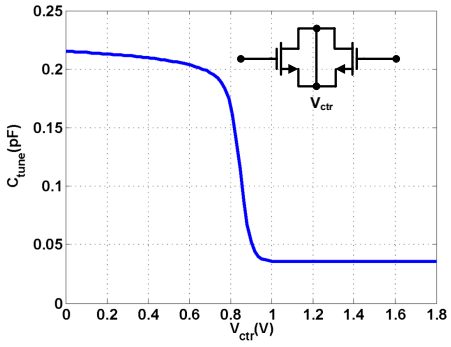

Fig. 6. The simulated tuning characteristic of two back-to-back on-chip NMOS varactors ($5\mu m \times 10\mu m$ each) in a 0.18μm CMOS process. The tuning ratio is $\sim$5.

to minimize initial capacitive loading to the FBAR tank, an efficient frequency tuning device is needed.

MOS capacitors are commonly used as tuning devices in integrated VCOs. Fig. 6 shows the simulated capacitance value for two back-to-back $5\mu m \times 10\mu m$ NMOS varactors in 0.18μm CMOS. In contrast, Fig. 7 is a simulated tuning

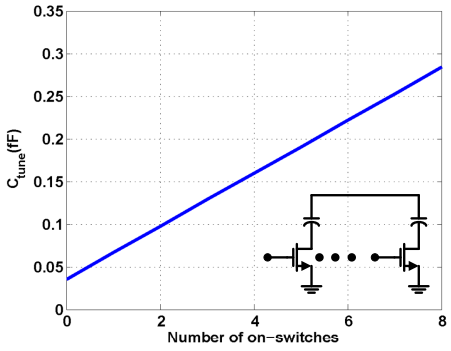

Fig. 7. The simulated tuning characteristic of digitally-controlled 3-bit capacitor array in a 0.18μ CMOS process. The unit capacitor is a 35fF MIM capacitor and the NMOS size is 6μm/0.18μ. The tuning ratio is 8.

curve of a switched 3-bit MIM capacitor array. An important measure of the quality of a tuning device is its tuning ratio C_{max}/C_{min}, where C_{max} and C_{min} are the maximum and minimum tunable capacitance. The simulated results presented in Figs. 6 and 7 show that the tuning ratio of the digitally switched capacitor array is much better than that of the analog varactor for our CMOS process and justify the use of digitally controlled capacitor arrays for frequency tuning, especially for FBAR oscillators where the parasitic capacitance loading must be strictly minimized.

A MIM capacitor generally has a relatively large minimum layout size (and thus capacitance value). This is undesirable for digitally controlled oscillator (DCO) frequency tuning as a large capacitive step size produces a coarse DCO frequency resolution. However, due to the low capacitance sensitivity of an FBAR oscillator, a relatively large unit capacitor can still produce a fine frequency resolution.

We propose to use the Pierce oscillator topology as shown in Fig. 8 for our wide-tuning FBAR oscillator. Compared to other classic Colpitts-like oscillator topologies, the feedback capacitors C_1 and C_2 in the Pierce oscillator can be readily replaced with the capacitor arrays controlled by the NMOS switches to realize digital frequency tuning.

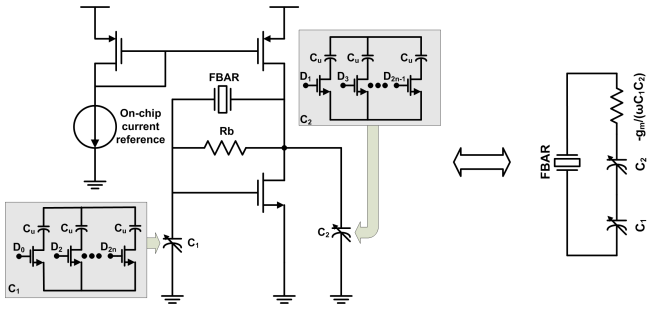

Fig. 8. The proposed FBAR-based oscillator and its equivalent small signal model (right). Two digitally-controlled MIM-capacitor banks are used to tune both C_1 and C_2. Thermometer coding and a staggered tuning scheme further enhance the frequency resolution, gain linearity, and tuning range of the digital FBAR oscillator.

In a PLL, the FBAR DCO must have reasonable linearity and a fine resolution for improved frequency spur and phase noise performance. We use thermometer coding for the digital control word D_i, i $\in \{1,2,...\ 2n\}$ and physically place two unit capacitors in close locations when their index numbers are close to each other to reduce the nonlinearity caused by process variation [11]. We alternately index the unit capacitors between the two banks to further improve resolution.

In a PLL, frequency tuning quantization of the DCO introduces additional quantization-induced phase noise. The quantization noise should typically be suppressed to make it negligible in comparison to the oscillator phase noise. The native phase noise of the DCO is determined by the resonator Q and signal power, which are governed by Leeson's model [12].

The quantization-induced phase noise can be approximated by [13] :

$$L(\Delta f) = \frac{1}{12}\frac{\Delta f_{res}}{\Delta f}^2 \frac{1}{f_R} sinc(\frac{\Delta f}{f_R})^2 . \quad (5)$$

where f_{res} is the DCO frequency resolution and f_R is the PLL reference frequency.

In Fig. 9, for the same tuning range (10MHz with carrier frequency 1.56GHz in this simulation), a DCO with a 14-bit frequency resolution is 36dB better in quantization-induced phase noise than an 8-bit DCO. From the simulation plot, we observe that the required frequency resolution must have at least 14 bits in order for the quantization noise to be below -100 dBc/Hz at 10kHz frequency offset, which is comparable to previously demonstrated native phase noise in [5][4][3].

In our CMOS process, there is a design rule constraint on the smallest implementable MIM capacitor. This limits the bit width of the DCO to 8. Moreover, a larger bit width digital control increases layout complexity, increases parasitic capacitance load from routing wires, and reduces the achievable

tuning range of the DCO. Fig. 10 shows a frequency dithering

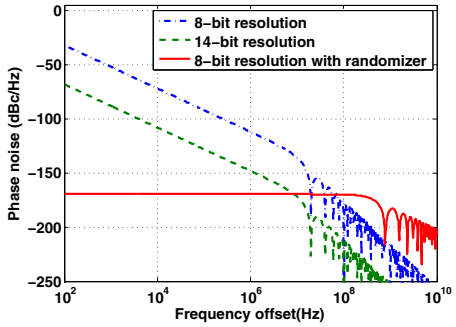

Fig. 9. Calculated DCO phase noise contributed by frequency quantization. A 20 MHz reference frequency (f_R) and tuning range of 10 MHz at 1.56 GHz carrier are assumed. The phase noise is 36 dB lower when the frequency resolution is increased from 8 bits to 14 bits. A first order $\Delta\Sigma$ frequency dithering at 1/2 carrier frequency can effectively increase frequency resolution from 8 bits to a required 14 bits.

technique that can be used to suppress quantization-induced phase noise. In this scheme, frequency resolution is improved by dithering a switch that controls a unit capacitor in the DCO in a randomized manner with an average temporal on-value equal to the specified input digits. The simulated phase noise for an 8-bit DCO that uses a first-order $\Delta\Sigma$ modulator as a randomizer is plotted for comparison in Fig. 9. With a 6-bit accumulator updating at half of the DCO frequency, the quantization-induced phase noise can be suppressed to a negligible level.

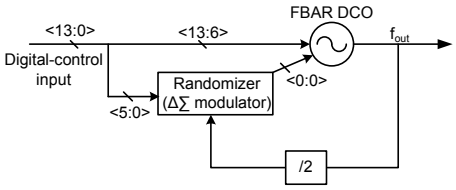

Fig. 10. Schematic of a frequency dithering technique. Frequency resolution of the DCO is improved by fast switching a unit capacitor in the DCO in a randomized manner with an average temporal on-value equal to the specified input digits.

IV. Experiment Results

The oscillator was fabricated in a 0.18μm CMOS process, occupying (720×850)μm^2 of chip area including the pads. The die photo is shown in Fig. 11.

The measured FBAR DCO tuning characteristic is shown in Fig. 12 at a current consumption of approximately 2.1mA. The power supply of the chip is 1.8V. The measured tuning range is 7250 ppm, which is the highest of any low power FBAR oscillator reported to date.

The bit width of the digital control word of the DCO is 8 (0 to 255 full scale). At the nominal bias current of 2.1mA, the oscillator is functional up to a code of 213, where the capacitive loading degrades the tank impedance enough to quench the oscillation.

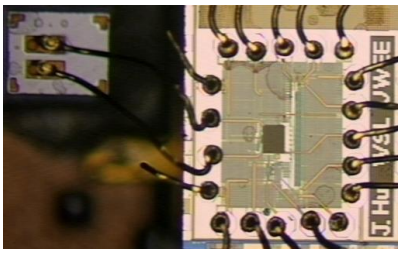

Fig. 11. Oscillator die photo. The FBAR die is on the left. On the right is the oscillator fabricated in a 0.18μm CMOS process with an area of (720×850)μm^2.

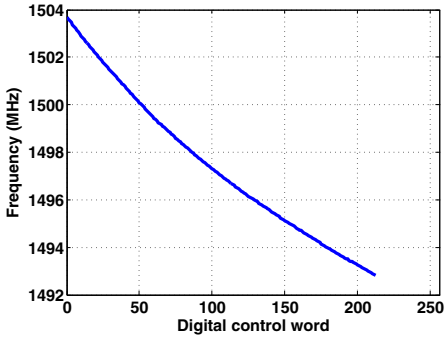

Fig. 12. Measured DCO tuning characteristic. The total tuning range is 7250 ppm.

The measured result in Fig. 12 shows that the DCO tuning gain decreases as the value of the control word increases. This is consistent with Equation 2. The nonlinearity of the DCO gain can be reduced if desired by tapering up the capacitor values of a thermometer-encoded capacitor array [11].

The measured phase noise is presented in Fig. 13. The achieved phase noise at 10kHz and 1MHz frequency offsets are 99dBc/Hz and 142dBc/Hz respectively.

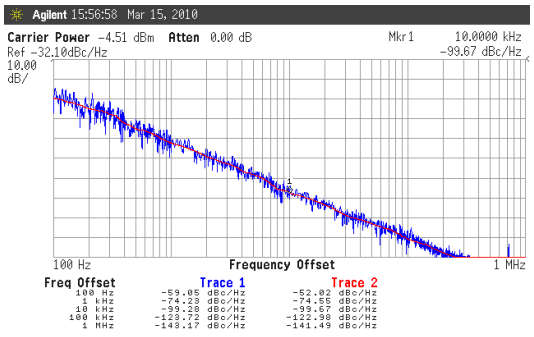

Fig. 13. Measured phase noise performance of the FBAR DCO using an Agilent E4440 PSA.

V. Conclusions

We have presented a digitally-controlled FBAR oscillator that achieves a tuning range over 8x better than previously published low power FBAR oscillators. A switched-MIM capacitor array is used for frequency tuning. The increased

tuning range allows the oscillator to be used in either a closed-loop all-digital PLL or as a free-running RF frequency reference for high speed ADCs, mm-Wave circuits, and high speed links. A performance summary and result comparison is given in Table I.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	this work	[5]
Process	CMOS 0.18μm	CMOS 0.13μm
Voltage supply (V)	1.8	1.0
Power consumption	3.78	0.6
Center frequency (GHz)	1.50	1.575
Phase noise @ 1kHz (dBc/Hz)	-82	-60
Phase noise @ 10kHz (dBc/Hz)	-99	-90
Phase noise @ 100kHz (dBc/Hz)	-123	-119
Phase noise @ 1MHz (dBc/Hz)	-142	-140
Tuning range (ppm)	7250	857

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