A 1.5GHz 0.2ps\textsuperscript{RMS} Jitter 1.5mW Divider-less FBAR ADPLL in 65nm CMOS

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Abstract—This paper presents a low power, low jitter, PVT-stable film-bulk acoustic wave resonator (FBAR) based all digital phase-locked loop (ADPLL) in a 65nm CMOS process. We introduce a power-efficient integer-N ADPLL architecture, where the digitally-controlled FBAR oscillator (FBAR DCO) achieves phase-lock to a reference clock without any explicit frequency dividers in the feedback path. The simplified divider-less ADPLL has a reduced phase difference at the input of the phase-frequency detector, avoiding a lengthy power hungry time-to-digital converter (TDC). The ADPLL consumes 1.5mW of power and has a measured integrated RMS jitter 0.19ps from 10kHz to 40MHz frequency offset at 1.5GHz carrier frequency. The measured frequency tuning range of 6300ppm for this ADPLL is wide enough to cover the FBAR frequency variations over PVT and provide moderate frequency modulation or channelization.

This low power high performance FBAR ADPLL can be used in low power radios, high performance ADCs, and high speed data links.

I. INTRODUCTION

Low power and low noise RF frequency synthesizers are essential for applications such as high performance ADCs, high speed serial data links, and low power radios [1] [2]. Film-bulk acoustic wave resonators (FBARs) show an enormous opportunity in low power high performance RF frequency generation, as they have a quality factor over 100 times higher than on-chip inductors and the potential for wafer- or package-level integration with mainstream CMOS [3] [4] [5].

In a PLL, the VCO and frequency dividers are typically the most power hungry blocks. It has been demonstrated that the phase noise of an FBAR VCO is significantly less than an LC VCO for comparable power consumption [3]. Thus, the relative power and noise contribution of the dividers becomes higher in an FBAR PLL.

Typically, a PLL uses a frequency divider in the feedback path. Previous work including [6] [7] demonstrated divider-less PLL concept using aperture phase-detection and subsampling. In these designs, auxiliary loops have to be designed to assist the main loop (the divider-less loop) to acquire the desired locking frequency during the initial phase acquisition stage. The auxiliary loop, which has frequency dividers in its feedback path, sets the VCO to a desired phase and frequency before the main loop is switched in. The main loop is engaged in a later stage in the locked state, achieving low phase noise and low power operation.

In this paper, we propose a divider-less all digital PLL architecture to further improve phase noise and power performance of FBAR ADPLLs [4]. In an FBAR PLL, since

![Fig. 1. The proposed divider-less FBAR ADPLL architecture.](image)

the FBAR oscillator has a limited frequency tuning range (typically less than 10,000ppm), the PLL is tunable within 20MHz, which presents a maximum of one frequency multiple when the reference frequency is above 20MHz. An FBAR PLL can be divider-less without an auxiliary locking circuit since the reference frequency can be readily made larger than the frequency tuning range of the FBAR oscillator.

This paper describes the architecture of the new divider-less all digital FBAR PLL. By eliminating the divider, the ADPLL reduces to a simplified architecture in which phase-detection can be realized with high resolution at a low power cost because of the reduced phase difference to be measured by a time-to-digital converter (TDC). Section II introduces the proposed ADPLL architecture. Section III describes the phase detection in the ADPLL. The experimental results are given in Section IV.

II. THE PROPOSED FBAR ADPLL ARCHITECTURE

FBAR oscillators have been shown to have a wider tuning range when digitally-tuned with a switched capacitor array compared to the analog tuning with a MOS varactor [4]. The proposed divider-less all digital FBAR PLL uses the DCO described in [4] in order to achieve a wide tuning range demanded for PVT variations and required for frequency modulation and channelization. The architecture of the ADPLL is shown in Figure 1. Since the FBAR DCO has low phase noise and low power consumption due to its high quality factor [3], we eliminate the frequency divider, which generally exists in a PLL feedback path, to further reduce power and phase noise originated from the divider.

The ADPLL comprises a re-sampling flip-flop (FF), a digital phase detector, a programmable digital loop filter (LF), and an FBAR DCO. The DCO output is re-sampled using the resampling FF which has the DCO output frequency $f_o$ driving
its clock input and the reference frequency \( f_{\text{ref}} \) at its data input. The FF generates a Late signal that runs at the same frequency as \( f_{\text{ref}} \) (Early), but is phase-synchronized with the DCO output \( f_o \). The timing diagram is given in Fig. 2. The timing difference \( d \) between Early and Late is equal to the timing difference between \( f_{\text{ref}} \) and \( f_o \), which is within one period of the DCO output \( T_o \). Since Late is the output of the re-sampling FF, the rising edge of Late signal is always later than the Early signal. Thus, the timing duration that a phase-detector needs to measure is within one period of the DCO \( T_o \), i.e., \( 0 \leq d \leq T_o \). With limited tuning range from the DCO, the timing uncertainty of the coming rising edge of the DCO is limited. Therefore, the phase difference between the reference clock and the feedback clock which the phase detector is required to detect is significantly reduced in this high Q PLL, leading to a power-efficient ADPLL architecture which is not required to have a power hungry phase accumulation operation typical in an ADPLL [8].

The phase detector includes an inverter-based TDC in which the inverter outputs are latched by the Late signal. The TDC resolution is one inverter delay (around 10ps in our 65nm CMOS process), which allows an estimated in-band quantization phase noise floor below -100dBc/Hz. The LF is realized with 2 IIR filters [8]. It is programmable through a serial interface with an adjustable loop gain from 10kHz to 100kHz. The FBAR DCO is a Pierce oscillator tuned with a switched capacitor array (128 thermometer-coded 26fF unit MIM capacitors). We use a first-order \( \Delta \Sigma \) modulator clocked at the rate of \( f_o/2 \) to implement the DCO frequency dither to obtain required frequency resolution for low noise operation [4].

III. PHASE DETECTION IN THE DIVIDER-LESS ADPLL

Fig. 3 shows the schematic diagram of the digital phase detector and its transfer function. The ratio of the locked DCO frequency to the reference \( f_o/f_{\text{ref}} \) is an integer \( N \). The phase error between the inputs (Early and Late) of the digital phase detector is thus between 0 and \( 2\pi/N \) measured in frequency \( f_{\text{ref}} \). We normalize the digital output from the TDC to 1 for a phase (timing) error of \( T_o \). The TDC output TDCout is a positive number which is proportional to the phase error \( \vartheta_e \) between Early and Late. We perform a linear transformation by adding a constant phase offset TDCos to the TDC output. The resulting transfer function of the phase detector PDout versus \( \vartheta_e \) possesses the characteristic of that in a type II PLL, i.e., PDout = 0 when \( \vartheta_e = 0 \), leading to a phase detector gain \( K_d = -N/2\pi \). An inaccurate delay estimation of the inverters in the TDC together with the TDC normalization can cause instability of the ADPLL. To overcome process variations, we design our loop with a large phase margin instead of spending energy for inverter delay scaling and shooting for a small phase margin [8].

In the transfer function curve of the phase detector (Fig. 3(b)), the span of PDout in the x-axis determines the frequency pull-in range of the PLL. The DCO has a tuning range that can create a maximum cumulative timing advance or lag of \( T_o \Delta f/f_{\text{ref}} \) within one period of the reference clock \( f_{\text{ref}} \), where \( \Delta f \) is the tuning range of the DCO. The PLL operates at the
origin of the PDout versus \( \vartheta_e \) curve when locked. The timing diagram is shown in Fig. 4. Hence, the PDout curve needs to extend in both directions of the x-axis in order to acquire the locking frequency from any point. Therefore, the TDC is required to have a minimum length of \( 2T_o \Delta f/f_{ref} \) for the PLL to lock to the full range of the DCO at any starting frequency, which is \( 2T_o \) at maximum assuming \( \Delta f < f_{ref} \). The programmable parameter TDCos is optimally set to the middle of the TDC. When locked, the TDC has a phase offset equal to TDCos. The non-zero phase offset between \( f_{ref} \) and \( f_o \) in the locked state is critical to the improved phase noise, as this reduces the likelihood of metastability occurring in the re-sampling FF.

IV. EXPERIMENTAL RESULTS

The design was implemented in a 65nm CMOS process. Fig. 5 shows the micrograph of the CMOS chip and the FBAR die. The FBAR is wire-bonded directly to the CMOS. The CMOS core occupies an area of \((0.2 \times 0.2)\text{mm}^2\). The ADPLL consumes 1.5mA current from a 1.0V supply (0.9mA digital, 0.6mA DCO).

The measured DCO tuning characteristic is given in Fig. 6. The DCO achieves a tuning range of 6300ppm. This tuning range is wide enough to stabilize the FBAR ADPLL over PVT variations and allow moderate frequency modulation (e.g. spread spectrum modulations in high speed data links) or channelization for RF transceivers.

The DCO has a 7-bit word of frequency control. We have built-in a frequency dither algorithm to provide additional 7-bit frequency resolution that is needed for the phase noise requirement in this design [4]. Fig. 7 shows the frequency output of the DCO versus time when it is locked to \( f_{ref} \). The frequency bounces around about 50ppm when the frequency dither is disabled, while it stays relatively stable (within 1ppm) when the frequency dither is enabled. The transient frequency measurement confirms the effectiveness of the frequency dither algorithm implemented in the design.

Fig. 8 shows the phase noise of the locked PLL overlaid on the measured phase noise of the free running DCO. The FBAR ADPLL achieves an integrated RMS jitter of 0.2ps from 10kHz to 40MHz. The in-band noise of the ADPLL is dominated by the 45 MHz reference clock (Agilent PSG-A Series Signal Generator E8254A). The best-case reference noise is -92.5dBc/Hz and -101.5dBc/Hz at 1kHz and 10kHz offsets, respectively, when referred to the 1.5GHz output. Better jitter performance could be obtained with a digital LF allowing a lower loop bandwidth.

The measured frequency spectrum of the ADPLL when it is locked is presented in Fig. 9. The observed reference spur is -44.6dBc.

A commonly used figure-of-merit (FOM) for frequency generation circuits is \( FOM = 10\log_{10}((\delta/\text{ppm})^2 P_{\text{ref}}) \), where \( \delta \) is the RMS jitter and \( P \) is the power consumption of the frequency reference [7]. Fig. 10 shows the FOM of the FBAR ADPLL in comparison with previously published
Fig. 9. The measured ADPLL output frequency spectrum.

Fig. 10. FOM comparison to previously published works.

Table 1 summarizes the performance of the FBAR ADPLL together with previously published works for comparison.

Table 1. Performance summary and comparison with previous works.

<table>
<thead>
<tr>
<th>PLL Type</th>
<th>Process (CMOS)</th>
<th>Carrier (GHz)</th>
<th>Ref. Spur (dBc)</th>
<th>Int. RMS Jitter (ps)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7] Sub-sampling LC analog</td>
<td>0.18µm</td>
<td>2.2</td>
<td>55</td>
<td>0.15</td>
<td>10k-40MHz</td>
</tr>
<tr>
<td>[9] Sub-sampling LC analog</td>
<td>0.18µm</td>
<td>2.21</td>
<td>55.25</td>
<td>0.3</td>
<td>10k-40MHz</td>
</tr>
<tr>
<td>[10] Fractional-N LC ADPLL</td>
<td>65nm</td>
<td>2.9-4.0</td>
<td>40</td>
<td>0.42</td>
<td>3k-30MHz</td>
</tr>
<tr>
<td>[11] Integer-N ring hybrid</td>
<td>65nm</td>
<td>1.21</td>
<td>55</td>
<td>0.57</td>
<td>1k-10MHz</td>
</tr>
<tr>
<td>This work FBAR ADPLL</td>
<td>65nm</td>
<td>1.508</td>
<td>45.697</td>
<td>0.19</td>
<td>10k-40MHz</td>
</tr>
</tbody>
</table>

V. CONCLUSIONS

We have introduced a 1.5GHz integer-N divider-less FBAR ADPLL in 65nm CMOS. The ADPLL has demonstrated a 0.19ps integrated RMS jitter from 10k to 40MHz frequency offset at 1.5mW of power. With its wide tuning range, the FBAR ADPLL offers a low power, low jitter PVT-stable RF frequency reference for high performance ADCs, high speed links, and low power wireless transceivers. The 5dB gain in FOM over the existing solutions is a great value proposition for the FBAR ADPLL to be used in battery-powered or battery-less wireless sensing devices where power consumption is strictly minimized while maximum data bandwidth is pursued.

REFERENCES