System Design Principles Combining Sub-threshold Circuits and Architectures with Energy Scavenging Mechanisms

Benton H. Calhoun, Sudhanshu Khanna, Yanqing Zhang, Joseph Ryan, Brian Otis[1]
Electrical and Computer Engineering, University of Virginia, Charlottesville, VA, USA
[1]Electrical Engineering, University of Washington, Seattle, WA, USA
<bcalhoun, sk4fs, yz4hz, jfr7p>@virginia.edu, botis@ee.washington.edu

***Abstract*—Ultra low power (ULP) circuits and energy scavenging mechanisms, though conceptually appealing, have been mainly studied in isolation to date. In this paper, we observe energy harvesting prototypes to derive system-level models and to reveal practical issues specific to various types of energy harvesting systems. Our models predict how design decisions affect overall lifetime. We use our model to derive system driven principles for optimizing architecture, voltage selection, and sub-threshold circuit designs across different types of power harvesting systems.**

INTRODUCTION

Wireless micro-sensors offer great promise for long term, comprehensive, inexpensive, and unobtrusive monitoring of a variety of environments. Size, weight, lifetime, and cost are the main metrics of interest for wireless micro-sensors. The desire for low cost and small size (e.g. <1cm^3) limits the amount of local energy storage (battery or capacitor), and the need to monitor over an extended lifetime translates this limited energy into a tight energy budget. The strict energy constraint makes sub-threshold circuit operation an ideal choice, since it minimizes energy per operation for digital computation [1]. Harvesting ambient energy offers an appealing alternative to battery-based operation. To sustain operation, the circuits in the node must consume less power than the energy harvesting mechanism produces or temporarily store energy for future use. In this paper, we examine the state-of-the-art for ULP circuits and for energy harvesting mechanisms and identify key principles for successful integration of the two into energy harvesting systems.

A variety of energy harvesting mechanisms exist, and the correct choice is highly application dependent. Industrial and aviation environments provide consistent vibrations, while body area sensors allow access to a reasonably consistent temperature gradient. Outdoor environments enjoy ample solar power, a modality that is well-studied in the literature and will not be discussed further here. Successful demonstrations of harvesting using these (and many more) modalities exist, but they generally produce fairly low power levels. For example, Figure 1 shows that most harvesting modalities struggle to provide 1mW within the desired size of a micro-sensor (e.g. <1cm^3). As a result, power available with energy harvesting usually is on the order of 50-100µW [3]. This fact points to some situations where battery power is preferred. For example, if the sensor size and weight specifications are not stringent, as in the case of a portable hospital health-monitoring basestation, a battery-only power source is simpler and more reliable and gives a lifetime limited only by cost. Another example is devices that only require sub-24 hour lifespans between re-charges (external hearing aids, for example).

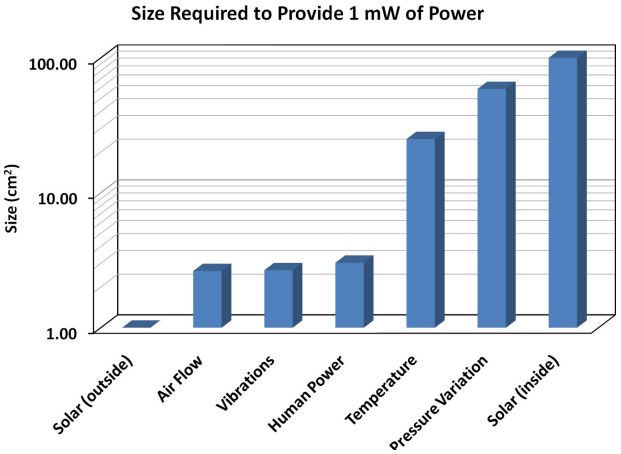

Figure 1: Approximate area required to provide 1mW from energy harvesting mechanisms.

To begin understanding how power harvesting affects the system design, we first define three broad types of energy scavenging systems. Type I – Harvesting as the sole power source. Type II – Harvesting in parallel with a primary battery. Type III – Harvesting with a chargeable battery. These three types of systems will impact the capabilities and design of the architecture and circuits. Figure 2 shows the possible structure of a harvesting chip for the three system types. The next two sections examine energy harvesting mechanisms and interface circuits, which will clarify how to design the three types of systems.

ENERGY HARVESTING MODALITIES

In this section, we introduce three power harvesting sources that have been successfully used to power our wireless systems [2][4][5]. These three power sources use

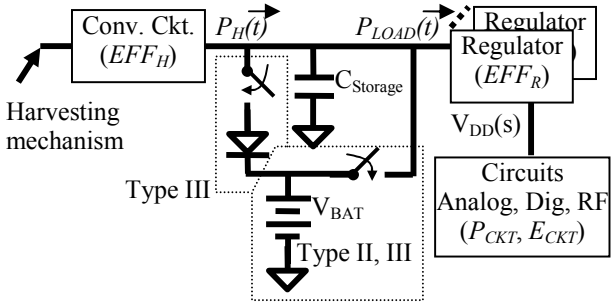

Figure 2: Generic power harvesting system diagram.

completely different harvesting mechanisms and present very different challenges to the circuit and system designer. We have utilized a $1cm^3$ vibrational harvester to power a 1.9GHz sensor-node transmitter [2]. Most recently, we have also used the small but ubiquitous voltage available from trees to power (0.2µW) a 1Hz oscillator and a boost converter [5]. Another illustrative example is shown below: thermoelectric power generation.

For wearable sensors, thermoelectric energy harvesting is a promising option. A thermoelectric generator (TEG) generates a voltage that is proportional to the difference of the temperatures applied to each side. One side is placed either on the warm skin or under the skin, while the other side is exposed to the cooler ambient air. Although the body temperature of the subject is well regulated, the ambient temperature, airflow, and thermal insulation due to clothing vary widely. Therefore, a DC-DC converter that can accommodate a widely-varying and low voltage source and boost it to a regulated supply is needed to operate low-power circuitry (e.g. [6]). Since our target sensing circuitry consumes 10µW of average power or less, the converter must have very low quiescent power consumption in order to efficiently drive the low-power load. An example of our hybrid solar/thermoelectric generator is given in Figure 3.

This hybrid power source uses four small silicon thermoelectric generators wired in series (50µW) as well as three photovoltaic solar cells. The power is combined and stored on a 22µF SMT capacitor. We have also fabricated a small (0.7cm x 1.5cm) PCB containing an off-the-shelf radio, MSP430 microcontroller, and nonvolatile memory. Experiments on these systems have revealed multiple challenges related to energy harvesting systems, which we will introduce and discuss in the next section.

Figure 3: Our prototype body-worn solar/thermo-electric generator for health monitoring applications.

ENERGY HARVESTING CHALLENGES

Our experiences with wireless sensor integration using harvested power have revealed three significant challenges.

First, energy harvesting sources present a very non-ideal supply voltage for the active electronics. Depending on the source, they suffer from widely varying output voltages, high source impedances, large ripple, and extremely low (sub-100mV) voltage levels. This requires non-standard boost converter architectures to allow conversion of low voltages to stable supply rails for digital logic and analog systems (e.g. [6]).

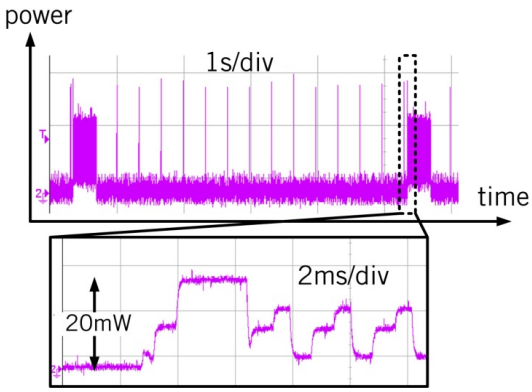

Figure 4: Measured power trace for our Encounternet sensor network boards. The inset shows the significant peak power levels during receive and transmit.

Second, high peak current levels cause significant voltage drops in high-impedance energy harvesting sources or small batteries. An example of a measured power trace for our prototype wireless sensor PCB is shown in Figure 4. Peak current levels in commercial transceivers are on the order of 10-30mA. This means that, even if the duty cycle is decreased arbitrarily to reduce the average power dissipation, these current levels are incompatible with small watch and hearing aid batteries. These current levels require inordinately large capacitors (on the order of 1mF) for high impedance supplies. Custom integrated RF solutions can help, but peak current will still be a concern.

Third, the power output of energy harvesters is highly environment-dependent (e.g., Figure 1, solar). For example, the output of body-worn thermoelectric generators will fall to near-zero if insulated by clothing or operated in a hot environment. Wearable solar cells are useless at night. Wirelessly powered devices only operate in close proximity with a reader. Vibrational energy harvesters are not only sensitive to the amplitude of vibration, but the vibration frequency as well. Thus, hybrid sources containing multiple energy harvesters are likely necessary.

SYSTEM DESIGN WITH ENERGY HARVESTING

The features of energy harvesting circuits from the previous sections indicate when the different types of harvesting mechanisms are appropriate. Type I systems run only from harvested energy, some of which can be stored locally on a capacitor (preferably on-chip for size and cost). Type I systems will be low cost and very small, so they may be ideal for integration into clothing in a body area sensor (hat-band, shirt, etc.). Limited energy storage means that large peak power surges may discharge the node's storage capacitor below a usable voltage. For this reason, and due to the unreliable nature of harvestable energy sources, Type I systems risk running out of energy and dying. Harvesting from a source capable of passively restoring operation (e.g. solar, RF) can allow them to re-start, but reliance on an active power circuit (e.g. thermoelectric) makes this node death permanent. The rest of this paper focuses on Type I systems. Type II systems add a non-rechargeable battery in parallel to the power harvesting. System requirements may require that this

method be used either to support operations with large peak current (e.g. long range RF transmission) or to increase reliability by operating during power harvesting blackouts. Once the battery fully discharges, the Type II system becomes Type I. Type III systems also have a back-up energy source to prevent node death. Since the battery inevitably holds more energy than an on-chip capacitor, the Type III node can tolerate long harvesting blackouts and then restore battery charge when harvesting resumes.

A. Energy Models

The Type I model must capture the fact that the available voltage on the capacitor (V_C) must remain large enough for the node to function, e.g. $V_C(t) > V_{KILL}$. To satisfy this condition over a long time, clearly the harvested power (P_H) must exceed the average consumed power:

$$P_H > P_{LOAD,AVG} \tag{1}$$

Also, for every given time period, the consumed energy must never exceed the usable stored energy ($E_{USE}=E_C-E_{KILL}$) on the capacitor:

$$\forall t, \quad E_{USE} \geq \int_0^t [P_{LOAD}(t) - P_H(t)]dt \tag{2}$$

Eq. (2) shows that load power can exceed P_H for some time so long as it does not deplete the stored energy. It is likely that (1) will not hold if the circuit is always operating due to small P_H. Thus, the circuit must operate in bursts, short enough to satisfy (2), followed by idle periods long enough to recover the V_C sufficiently to allow further operation and to ensure that (1) holds over time.

By analyzing the energy use of circuits on the chip and knowing the storage capacitance, C, we can compute the maximum duration of these bursts of operation. Without loss of generality, we will assume that a single regulator supplies a fixed V_{DD} to the circuits. The efficiency of the regulator (EFF_R) leads to $E_{CKT}=E_{LOAD}*EFF_R$. Each time the circuit consumes energy for one "operation," E_{CKT}, V_C decreases slightly. If P_H and EFF_R remain constant, the number of operations permitted before $V_C=V_{KILL}$ equals:

$$N = \frac{C(V_{CC}^2 - V_{KILL}^2)}{\frac{E_{CKT}}{EFF_R} - t_{CKT}P_H} \tag{3}$$

where V_{CC} is the maximum allowable voltage on C, and t_{CKT} is the delay of an operation. Figure 5 shows how N varies with regulated V_{DD} for digital operations, assuming a linear regulator and a switched cap (S-C) regulator tuned for low loads [7]. The $V_{DD\text{-}MIN}$ for the circuit may not be the point where N is maximized; if P_H exceeds leakage power, P_{LK}, the total energy "lost" during an operation actually decreases as V_{DD} is lowered due to larger harvested energy over the slower operation time. If $t_{CKT}P_H > E_{CKT} / EFF_R$, then the circuit reaches equilibrium and $N=\infty$, as the top line in Figure 5 shows for the assumed value of P_H.

Type II systems share the same model as Type I for normal operation, but they are more reliable since they have a mechanism for restarting if the node dies while running on harvested power. The battery can also supply energy to allow violations of (2) for operations with large energy

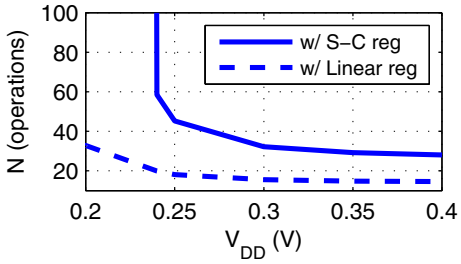

Figure 5: Number of "operations" achievable vs. regulated V_{DD} applied to the circuit.

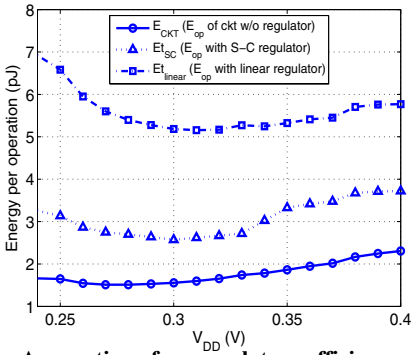

Figure 6: Accounting for regulator efficiency raises the optimum V_{DD} to maximize lifetime.

draws (e.g. RF transmission). The model for Type III turns out to be very similar to Type I. For example, both (1) and (2) apply exactly. The primary differences in a battery relative to a capacitor are that the battery has a larger storage capacity, and its voltage tends to remain more constant as its stored energy drops relative to a capacitor.

B. Design Principles for Energy Harvesting Systems

Now we examine methods to optimize a system for energy harvesting, focusing on Type I systems. First, we observe from (2) that we should maximize E_{USE} and P_H and minimize P_{LOAD}. We can maximize E_{USE} by using the largest capacitance possible, but this is limited by die space. We should also design the harvesting circuit to operate at the lowest voltage and energy possible to lower V_{KILL} and E_{KILL}.

Since P_{LOAD} is small for digital operation, the voltage regulator becomes quite important, as converter efficiency drops at low loads. To maximize (3), we consider both the minimum E_{CKT} of the load and the efficiency of the regulator. Figure 6 compares the total energy consumed per operation with both a linear regulator and the S-C regulator from [7]. The optimal energy point moves to a higher V_{DD} due to low EFF_R at low V_{DD} and low load power. Thus, it is important to design a regulator that is tuned for low loads. For harvesting systems, S-C regulators steal capacitance area away from the storage capacitor, but switching regulators may require large, costly off chip parts.

Some components of the circuit (e.g. RF or analog) may require a P_{CKT} that is much greater than P_H when they are active. Such energy hungry operations will not allow an intrinsic equilibrium point (e.g. Figure 5), so we must explicitly duty cycle, or intersperse idle periods between active operations, to meet (2). To do so, we must wait long

enough (t_{WAIT}) between operations so that harvested energy replaces the consumed energy (denominator of (3)):

$$t_{WAIT} \geq \frac{E_{CKT} / EFF_R - t_{CKT} P_H}{P_H - P_{LK-I} / EFF_R} \quad (4)$$

where P_{LK-I} is the leakage/static power during idle. Inserting a wait time from (4) allows N to become infinite, but t_{WAIT} could be large for large E_{CKT}. If we can power gate or otherwise reduce idle current so $P_H >> P_{LK-I}$, (4) becomes: $t_{WAIT} \geq t_{CKT}(P_{LOAD-AVG} - P_H)/P_H$. In this case, t_{WAIT} exceeds t_{CKT} by the ratio of dissipated and harvested power.

Since high power operations increase t_{WAIT}, sub-threshold digital circuits should be leveraged to reduce the demand for analog and RF components [8]. For micro-sensors, this method is most effective after determining what information must ultimately be derived from the raw sensed data. Often, focusing on the most efficient way to extract the information allows for substantial savings relative to individually optimizing each block's specification. For example, we have demonstrated a 0.13-µm CMOS mixed signal system-on-chip (SoC) that implements an electrocardiogram (ECG). The SoC includes an analog front end (instrumentation amp (IA) and analog to digital converter (ADC)) and a sub-threshold micro-processor [9]. The processor consumes only 1.5pJ at 280mV (0.7 uW), and we use it for signal processing and for controlling the analog circuits. This chip is ideal for monitoring for cardiac arrhythmias, whose presence can be identified by abnormalities in the heart rate, making full ECG transmission only necessary when actual arrhythmic events occur. By extracting the heart rate interval on chip, we can reduce the wireless data rate by over 500X, allowing for reduced use of a power hungry radio [9]. The heart rate algorithm can continue to operate accurately even when the analog components operate at lower voltages to save power. The SoC consumes only 2.6 µW while providing either computed heart rate or ECG data.

Sub-V_T operation lowers the power consumption of traditional digital systems down to a few µWs. By re-thinking the digital architecture, we can lower the power levels even further. In the sub-V_T region, serial architectures lower both active and leakage power [10]. While working at a given sub-V_T voltage, a 1-bit Serial Adder (SA) has 32x lower leakage power (Figure 7b) than a 32-bit Kogge-Stone Adder (KSA) at the cost of 11x higher delay [10]. Lower P_{LK-I} helps free up more power for and time for active operation on a limited P_H budget by enabling the storage capacitor to recuperate faster, e.g. (4).

For time critical operations, it is possible to increase the V_{DD} of a serial block while retaining its active and leakage power benefits [10]. Figure 7a compares a SA operating at a V_{DD} of 350mV with a 32-bit KSA at 200mV that have the same throughput. The figure shows the instantaneous power drawn (including clock and flop power) while both topologies carry out a 32-bit add operation at equal speed. The SA lowers $P_{LOAD,AVG}$ and also smears out the large peaks in the KSA current waveform. Thus, serial architectures help lower both $P_{LOAD,AVG}$ and $P_{LOAD,PEAK}$. Lower peak power at the component level translates to lower peaks at the system level, and thus can help ease regulator design and reduce decap requirements.

CONCLUSIONS

To make an efficient system working off harvested energy, co-design of the energy harvesting mechanism and the processing circuitry is essential. We have presented a model for estimating processing capability based on available harvested power, storage capacitor size, active and leakage power, and regulator. This model informs decisions about the appropriate regulator, architecture, and voltages for a given harvesting application. Since regulator efficiency decreases with V_{DD}, the optimal V_{DD} increases somewhat from the optimal V_{DD-CKT}. Leveraging sub-threshold digital operation can reduce the use of higher power analog and RF. Serializing the architecture helps lower energy and average power, and it smears the peak power, thus enabling longer lifetime and smaller decap. Based on characteristics of sub-threshold digital operation, regulators with higher efficiency at low load, and a standby mode would be useful in improving processing capability.

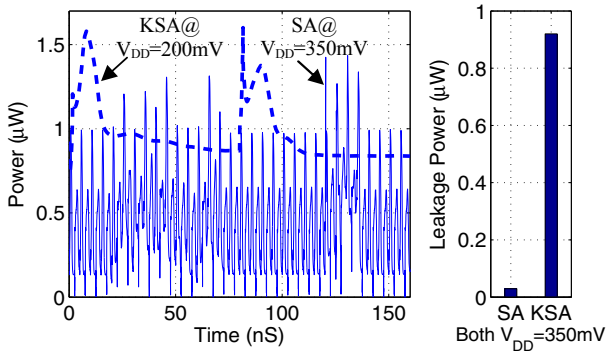

Figure 7: (a) Serial architectures provide lower P_{ACT} and P_{PEAK} at the same speed as parallel and (b) reduce P_{LK-I} substantially at the same V_{DD} (22nm PTM).

REFERENCES

[1] B.H. Calhoun, A. Wang, and A. Chandrakasan "Modeling and Sizing for Minimum Energy Operation in Sub-threshold Circuits," *Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1778-1786, 2005.

[2] S. Roundy, B. Otis, Y.H. Chee, J. Rabaey, P. Wright, "A 1.9GHz RF Transmit Beacon using Environmentally Scavenged Energy", *Int'l Symposium on Low Power Electronics and Design*, 2003.

[3] S. Roundy, et al., "Improving Power Output for Vibration-Based Energy Scavengers", *IEEE Pervasive Computing Journal on Mobile and Ubiquitous Computing*, vol. 4 , no. 1, March 2005, pp. 28-36.

[4] D. Yeager, J. Holleman, R. Prasad, J. Smith, B. Otis, "NeuralWISP: A Wirelessly-Powered Neural Interface with 1-m Range," Accepted, *IEEE Transactions on Biomedical Circuits and Systems*.

[5] C. Himes, E. Carlson, R. J. Ricchiuti, B. P. Otis, B. A. Parviz, "Ultra-Low Voltage Nanoelectronics Powered Directly, and Solely, from a Tree," Accepted, *IEEE Transactions on Nanotechnology*.

[6] E. Carlson, K. Strunz, B. Otis, "20mV Input Boost Converter for Thermoelectric Energy Harvesting," *Symp. on VLSI Circuits*, 2009.

[7] Y. Ramadass and A. P. Chandrakasan, "Voltage Scalable Switched Capacitor DC-DC Converter for Ultra-Low-Power On-Chip Applications," *Power Electronics Specialists Conference*, 2007.

[8] B. H. Calhoun, et al., "Sub-threshold Operation and Cross-Hierarchy Design for Ultra Low Power Wearable Sensors," *International Symposium on Circuits and Systems*, 2009.

[9] S. Jocke, J. Bolus, S.N. Wooters, A.D. Jurik, A.C. Weaver, T.N. Blalock, and B. H. Calhoun, "A 2.6-µW Sub-threshold Mixed-signal ECG SoC," *Symposium on VLSI Circuits*, 2009.

[10] S. Khanna and B. H. Calhoun, "Serial Sub-threshold Circuits for Ultra-Low-Power Systems," *ISLPED*, 2009.