A 90 μW MICS/ISM Band Transmitter with 22% Global Efficiency

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***Abstract*—For fully autonomous implantable or body-worn devices running on harvested energy, the peak and average power dissipation of the radio transmitter must be minimized. We propose a highly integrated 90 μW 400 MHz MICS band transmitter with an output power of 20 μW leading to a 22% global efficiency — the highest reported to date for such systems. We introduce a new transmitter architecture based on cascaded multi-phase injection locking and frequency multiplication to enable low power operation and high global efficiency. Our architecture eliminates slow phase/delay-locked loops for frequency synthesis and uses injection locking to achieve a settling time $<$ 250 ns permitting very aggressive duty cycling of the transmitter to conserve energy. At a data-rate of 200 kbps, the transmitter achieves an energy efficiency of 450 pJ/bit. Our 400 MHz local oscillator topology demonstrates a figure-of-merit of 204 dB.**

I. Introduction

In 1999, the FCC established the Medical Implant Communications Service (MICS) band to address the need for ubiquitous body area networks (BAN) comprising body-worn or implanted devices that continually sense vital body parameters [1]. Battery replacement for these devices may not be feasible or desirable, placing severe constraints on the power dissipation of the radio transceiver that tends to consume the bulk of total power. Other interesting applications enabled by ultra-low power radios are the animal tracking systems such as a moth flight recorder that requires payloads less than one gram [2]. High power dissipation in the radio will lead to a reduced recording time.

The typical power harvested from common surroundings is on the order of 100 μW [3]. Since the transmitter tends to dominate the total power budget, its power consumption needs to be below 100 μW. We report the first highly integrated 90 μW MICS band transmitter, realizing a significant improvement in the state-of-the-art. To achieve low power consumption without sacrificing performance, we introduce techniques both at the architecture and circuit level. Using cascacaded multi-phase injection locking and frequency multiplication, our local oscillator achieves a high figure-of-merit of 204 dB. Our architecture also helps eliminate the slow phase/delay locked loops used in carrier generation, and therefore permits agile duty cycling of the transmitter to conserve energy.

One significant challenge in the design of ultra-low power transmitters is the loss of global efficiency as the PA output power drops ($\leq$ 25 μW in the MICS band). The power dissipation in the carrier generation and data modulation circuitry constitutes a large percentage of total power consumption of the transmitter, leaving the PA efficiency as a secondary concern. As a result, the best reported global efficiency for MICS band transmitters is $<$6.5% [5]– [6]. This work presents a greater than 3$\times$ improvement in the global transmitter efficiency at 20 μW of transmit power.

II. Brief Literature Review

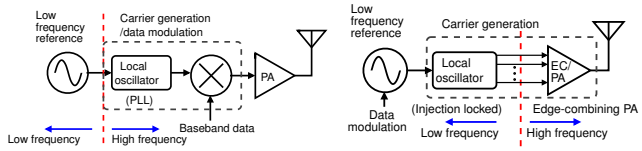

Fig. 1. (a) The conventional transmitter architecture (b) Proposed ultra-low power (ULP) transmitter architecture.

A number of integrated MICS band ultra-low power (ULP) transmitters have appeared in recent literature [4] [5] [6] [7]. In order to reduce the power consumption of the transmitter, the performance burden is shifted to a power hungry receiver. For example, to reduce power dissipation in carrier generation that typically dominates the total power budget in ULP transmitters, an open loop oscillator is used in [4] and [5]. The necessary frequency stability is obtained using a frequency correction/calibration loop running at the receiver. Others have adopted an RFID-style passive tag to perform medical sensing [8]. This again requires a power hungry RFID receiver. In summary, all the low-power transmitters described above shift the performance burden to a complex receiver resulting in high energy per *transceived* bit. This results in a highly asymmetrical link unsuitable for autonomous peer-to-peer body area network applications running on scavenged energy. Authors in [7] attempt to reduce the energy per bit by operating at higher data rates. However, small implantable batteries and scavengers typically exhibit a large source resistance that may not be able to supply the large peak currents needed for such systems. It is therefore desirable to achieve a sub-100 μW of power dissipation in the transmitter *without* introducing asymmetry in the radio link to enable the true autonomous medical sensing and telemetry.

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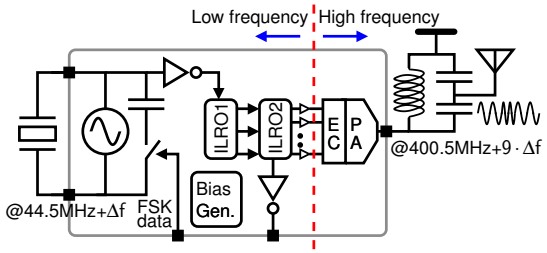


Fig. 2. Detailed block diagram of the proposed transmitter architecture for ultra-low power operation.

III. Proposed Architecture

Conventional ULP transmitters perform frequency synthesis and data modulation at the carrier frequency leading to poor global efficiency and high power consumption (Figure 1(a)). Our proposed transmitter achieves very low power dissipation by performing these operations at a much reduced frequency and employing an edge-combiner merged into the power amplifier (PA) (Figure 1(b)). However, in order to obtain the equally spaced edges necessary for the edge-combiner, a delay chain or a ring oscillator locked in a PLL/DLL is needed. The additional components in the loop such as charge-pump and loop filter present significant area/power overhead, while the settling time of the loop constrains the maximum possible duty cycling of the transmitter [6]. Any attempt to directly injection-lock the multi-phase low-frequency ring oscillator using the single phase crystal reference will introduce significant mismatches in the delayed waveforms of the RO. We address this issue by using cascaded injection-locking (Figure 2). The proposed architecture is an example of digitally-assisted RF design that benefits from CMOS and power supply scaling. The key building blocks of our proposed architecture — the edge-combining PA, the injection-locked oscillator and data modulation — are described below:

A. Edge-combiner

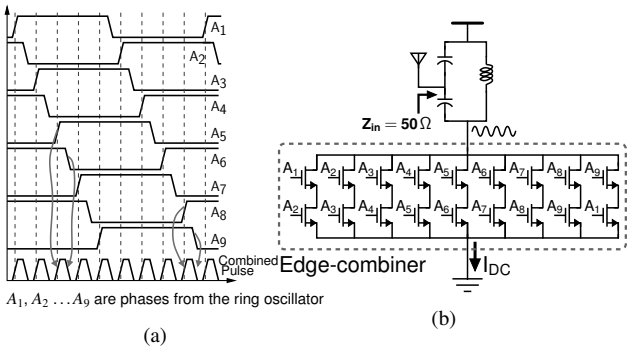


Fig. 3. (a) The principle of edge-combining (b) Schematic of the edge-combiner.

The low-power frequency multiplier is based on the principle of edge-combining. Let $A_1, A_2 \ldots A_N$ be the waveforms from a digital ring oscillator running at frequency f_{RO}. The waveform $\Sigma(A_1A_2 + A_2A_3 \ldots A_NA_1)$ is a square wave of frequency Nf_{RO} where N is both the factor of multiplication and the number of stages in the ring oscillator. For our 9-stage ring oscillator, the waveforms $A_1, A_2 \ldots A_9$ are spaced apart by a period of $T/18$, where T is the time period of the reference input at 44.5 MHz (Figure 3(a)). We use MOS transistor switches to perform an AND operation and sum the switched currents to realize an OR operation (Figure 3(b)).

We take advantage of low output power requirement of the MICS standard to combine the PA functionality with the edge-combiner which behaves like a non-linear power amplifier (Figure 3(b)). The load impedance of the edge-combiner is transformed using a tapped-capacitor matching network to match a 50 Ω antenna. This high-Q load at the edge-combiner output also attenuates the out-of-band spurs resulting from the mismatches in the low-frequency ring oscillator.

B. Injection-locked LO Design

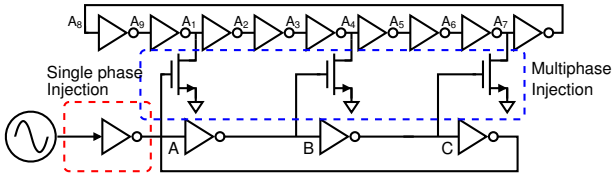


Fig. 4. Schematic of the two-stage multi-phase injecton-locked ring oscillator.

To ensure frequency stability across PVT variations, we injection-lock the low-frequency ring oscillator to an on-chip crystal reference, thereby eliminating the need for a PLL. The fast lock-time (on the order of 250 ns) of the LO allows aggressive duty cycling of the transmitter to further save power. Figure 4 shows the schematic of the 3-phase 2-stage injection-locked oscillator. The first stage of injection locking by the crystal oscillator ensures the correct frequency and low phase noise. However, the single-phase injection introduces asymmetry in otherwise equally spaced phases (A, B and C) of the ring oscillator. This asymmetry will lead to large reference spurs in the frequency multiplied output. The second stage of injection-locking attenuates this phase imbalance by using 3-stage symmetrical injection in a 9-stage ring oscillator. As shown in [9], cascaded multiphase injection-locked oscillators can be used to correct the phase and amplitude mismatches. The phase mismatches in phases $A_1, A_2, \ldots A_9$ are approximately an order of magnitude smaller than those in A, B and C. Multiphase-injection locking also increases the locking bandwidth ensuring reliable operation across PVT variation.

C. Data Modulation

On-chip FSK modulation is accomplished by pulling the quartz reference clock. The resulting frequency deviation is multiplied by 9×. Presence of crystal shunt capacitance C_0 and parasitic capacitance C_p in the circuitry limits the maximum fractional pulling to about a few hundred ppm. For a 44.5 MHz crystal, we obtained >20 kHz of frequency pulling, resulting in a 180 kHz frequency deviation about the carrier frequency.

IV. Measurement Results

This section presents the measured results from our 400.5 MHz transmitter prototype, implemented in 130 nm CMOS, based on the architecture described above. The entire system is integrated except for the crystal and the matching network. Figure 5 shows the frequency multiplied output at -17 dBm output power. The carrier-to-spur ratio (CSR) is 42.77 dB indicating excellent matching in phases $A_1, A_2, \ldots A_9$.

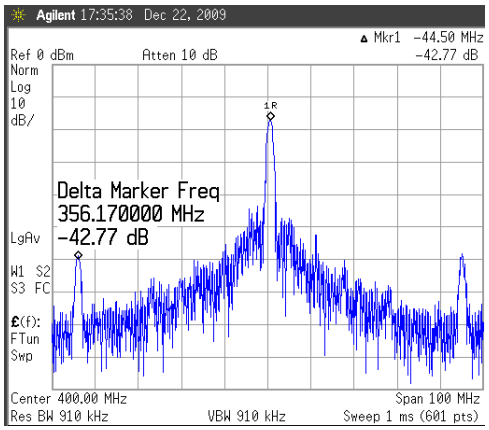
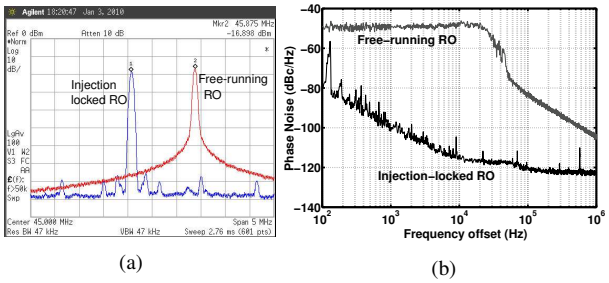


Fig. 5. Measured carrier-to-spur ratio of 42.77 dB was achieved.

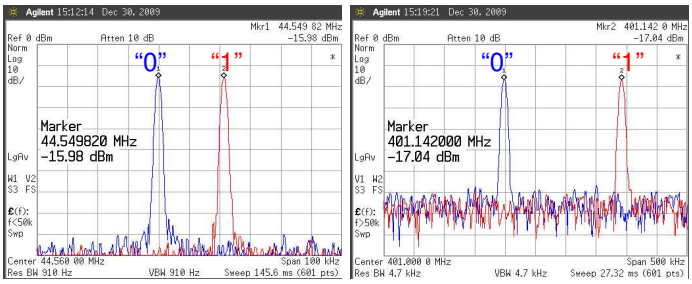
Figure 6(a) shows the overlaid spectrum of the free running and the injection-locked ring oscillator. As shown in Figure 6(b), the close-in phase noise of the injection-locked ring oscillator is vastly improved. The locking range of the 45 MHz free-running ring oscillator extends from 32–52 MHz (44% locking bandwidth). This allows operation in the 433 MHz ISM band using a 48 MHz crystal. The FSK modulated waveforms of the locked oscillator and the frequency multiplied output are captured in Figure 7. An FSK modulated pseudo-random data sequence was successfully detected using a commercial off-the-shelf receiver at a data rate of 200 kbps.



(a) (b)

Fig. 6. (a) The spectrum and (b) the measured phase noise of the free running and the injection-locked ring oscillator.

Figure 8 presents the phase noise of the injection-locked ring oscillator and the frequency multiplied output. At a given offset, the phase noise of the frequency multiplied output is higher than that of the 44.5 MHz ring oscillator by $20\log_{10}(9) \approx 19$ dB. At 300 kHz offset, the frequency-multiplied output achieves a phase noise of -105.2 dBc/Hz.



(a) (b)

Fig. 7. (a) FSK modulated 44.5 MHz injection-locked ring oscillator. $\Delta f_{RO} = 20$ kHz (b) FSK modulated frequency multiplied output at 400.5 MHz. $\Delta f_{RO} = 180$ kHz

The oscillator figure-of-merit (FoM) is given as

$$\text{FoM(dB)} = -\mathcal{L}(\Delta\omega) + 20\log\left(\frac{f_0}{\Delta f}\right) - 10\log(\text{P(mW)})$$

For our 400.5 MHz frequency multiplied oscillator, the FoM is 204 dB.

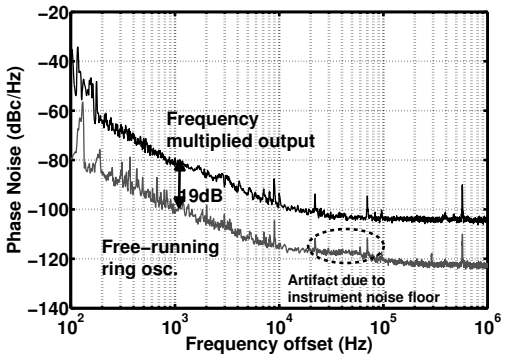


Fig. 8. Measured phase noise of the injection-locked LO and the frequency multiplied output using an Agilent E4446A spectrum analyzer.

Using our proposed techniques of high efficiency frequency multiplication and multi-phase cascaded injection locking, we were able to reduce the total power dissipation in carrier generation and data modulation to less than 24 μW. The measured PA drain efficiency is higher than 30% for an output power greater than 20 μW (Figure 9).

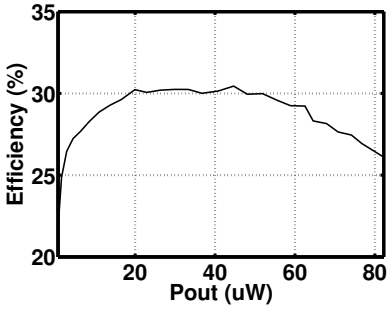


Fig. 9. Measured PA drain efficiency

Figure 10 presents the measured input return loss for the transmitter. Excellent matching with a measured $|S_{11}|$ <-22 dB was achieved.

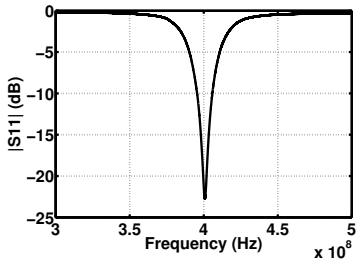


Fig. 10. Measured input return loss. $|S_{11}|$ <-10 dB.

Figure 11 shows the chip micrograph of the die, implemented in 130 nm CMOS. Due to the highly digital architecture of the proposed transmitter, and the absence of the synthesizer loop along with its large loop filter capacitors, the active area is less than 200 μm × 200 μm.

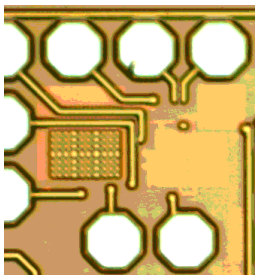


Fig. 11. The chip micrograph of the ultra-low power transmitter. The active area of the transmitter is ≈ 200 μm × 200 μm.

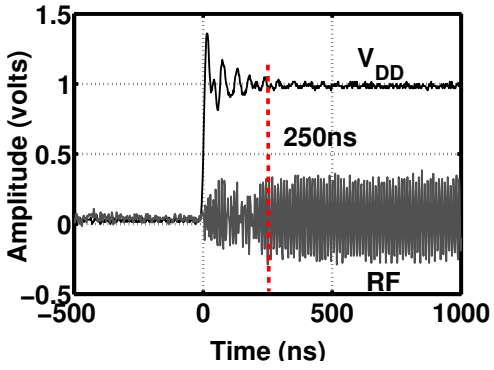


Fig. 12. A settling time <250 ns was measured.

Due to the absence of a PLL, Figure 12 shows a transmitter start-up time less than 250 ns. Table I captures the summary of the latest reported transmitters for the MICS band, along with our proposed work. Our transmitter has a global efficiency of 22% and energy efficiency of 450 pJ/bit which is a 3× improvement in the state-of-the-art.

TABLE I
PERFORMANCE SUMMARY OF THE ULP TRANSMITTERS AND THE PROPOSED TRANSMITTER

	[4]	[7]	[5]	[6]	**This Work**
Power dissipation	350 μW	5 mW	400 μW	400 μW	**90 μW**
Data-rate	120 kbps	800 kbps	250 kbps	100 kbps	**200 kbps**
Transmit power	NA	-4 – -17 dBm	-16 dBm	-16 dBm	**-17 dBm**
Energy per bit	2.9 nJ/bit	6.3 nJ/bit	1.4 nJ/bit	4 nJ/bit	**0.45 nJ/bit**
Process	90 nm	180 nm	130 nm	130 nm	**130 nm**
Modulation	MSK	FSK	FSK	FSK	**FSK**

V. CONCLUSION

We report the first sub-100μw MICS band transmitter with 22% global efficiency and 450 pJ/bit energy efficiency at a data-rate of 200 kbps. Using the techniques of cascaded multiphase injection-locking and frequency multiplication, we perform carrier generation without the slow phase/delay locked loops which allow a settling time <250 ns. Except for the crystal and the matching network, the entire transmitter is integrated with an active area less than 200 μm × 200 μm. The 400 MHz LO is locked to a crystal reference and achieves a FoM of 204 dB.

ACKNOWLEDGMENT

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REFERENCES

[1] http://wireless.fcc.gov/services/index.htm?job=service_home&idmedical_implant

[2] B. Otis, C. Moritz, J. Holleman, A. Mishra, J. Pandey, S. Rai, D. Yeager, F. Zhang, "Circuit techniques for wireless brain interfaces, " *IEEE Conf. on Engineering in Medicine and Biology Society, 2009* pp. 3213–3216, Sept. 2009

[3] S. Roundy, E.S. Leland, J. Baker, E. Carleton, E. Reilly, E. Lai, B. Otis, J.M. Rabaey, P.K. Wright, V. Sundararajan, "Improving power output for vibration based energy scavengers," *IEEE Pervasive Computing*, vol. 4, no. 1, pp. 28–36, Jan. 2005

[4] J. Bohorquez, A. Chandrakasan, J. Dawson,"A 350 μW CMOS MSK transmitter and 400 μW OOK super-regenerative receiver for medical implant communications," *IEEE Journal of Solid-State Circuits,* vol. 44,no. 4,April 2009 pp. 1248–1259

[5] J. Bae, Namjun Cho, H.-J. Yoo, "A 490 μW fully MICS compatible FSK transceiver for implantable devices," *IEEE symposium on VLSI Circuits,* June 2009

[6] S. Rai, J. Holleman, J. Pandey, F. Zhang, B. Otis, "A 500 μW neural tag with 2 μV_{rms} AFE and frequency-multiplying MICS/ISM FSK transmitter," *IEEE International Solid-State Circuits Conference*, Feb. 2009

[7] P. Bradley, "An ultra low power, high performance medical implant communication system (MICS) transceiver for implantable devices," *IEEE Biomedical Circuits and Systems (BioCAS)*, 2006

[8] D.J. Yeager, J. Holleman, R. Prasad, J.R. Smith, B.P. Otis,"NeuralWISP: a wirelessly powered neural interface with 1 m range," *IEEE Trans. on Biomedical Circuits and Systems,* vol. 3, no. 6, Dec. 2009 pp. 379–387

[9] P. Kinget, R. Melville, D. Long, V. Gopinathan, "An injection-locking scheme for precision quadrature generation," *IEEE Journal of Solid-State Circuits,* vol. 37, no. 7, July 2002 pp. 845–851