A Digitally Compensated 1.5 GHz CMOS/FBAR Frequency Reference
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Abstract—A temperature-compensated 1.5 GHz film bulk acoustic wave resonator (FBAR)-based frequency reference implemented in a 0.35 μm CMOS process is presented. The ultra-small form factor (0.79 mm × 1.72 mm) and low power dissipation (515 μA with 2 V supply) of a compensated FBAR oscillator present a promising alternative for the replacement of quartz crystal frequency references. The measured post-compensation frequency drift over a 0–100°C temperature range is <±10 ppm. The measured oscillator phase noise is −133 dBc/Hz at 100 kHz offset from the 1.5 GHz carrier.

I. INTRODUCTION

Even a cursory glance at different existing electronic applications highlights the need for a clock source in nearly every system. Quartz crystal tuned oscillators (XOs) are the industry standard for portable clock applications. Their superior frequency accuracy, low frequency drift with temperature and low noise allow quartz oscillators to dominate the commercial market. But while the density of electronics has grown exponentially as predicted by Moore’s law, the physical size of the quartz crystal has not scaled accordingly. Fig. 1 shows a self-contained wireless sensing node module, revealing that the physical size of quartz crystals has become comparable to integrated electronics. For miniaturized wireless systems, some of which demand completely thin-film integration of all components, there is need for a quartz alternative that has a small form factor while providing integration possibilities with commercial CMOS processes. An example of a commercial crystal XO datasheet suitable for wireless standards like Bluetooth and WLAN can be found in [1]. These wireless systems require ±20 ppm frequency stability over a 100°C temperature range, power supply variations, load changes, and other environmental variations. The commercial XO in [1] has a measured maximum integrated phase jitter of 1 ps rms for a 10 kHz to 20 MHz frequency band. We will explore the feasibility of electrically compensating a film bulk acoustic wave resonator (FBAR)-based oscillator for frequency drift over a 100°C temperature change while achieving acceptable phase jitter for wireless systems.

This work presents a temperature-compensated 1.5 GHz FBAR-based frequency reference with ±10 ppm frequency drift over a 0 to 100°C temperature range. The temperature-compensated zero drift resonator (ZDR) FBARs fabricated at Avago Technologies demonstrate a best case ±20 ppm to a worst case ±80 ppm total frequency drift, measured at the series resonance over a 0 to 100°C temperature range. The temperature range over which we can achieve this stability is determined by the choice of turn-over temperature (TOT) and the residual quadratic term, β, of the acoustic stack. TOT and β are set by the temperature coefficient of frequency (TCF) of the temperature compensating oxide layer (positive) used in the ZDR, the relative thickness of this oxide layer, and the relative thickness of the piezoelectric layer and electrode layers (both of which have a negative TCF). The TOT can be set as low as −20°C to as high as 100°C (the quadratic β term varies slightly as a function of TOT). The frequency of these ZDR devices is 1.5 GHz, fabricated according to GPS filter and S-ATA specifications, and are chosen in this work to demonstrate electrical compensation of FBAR-based oscillator. The divided frequencies in the 10 to 150 MHz frequency range can be used for quartz replacement in future systems.

Various quartz alternatives are discussed in Section II. Section III provides a direct comparison of FBAR with on-chip LC tanks as a tuning element. Section IV introduces design considerations for a temperature-compensated FBAR/CMOS frequency reference, followed by measurement results in Section V.

II. QUARTZ ALTERNATIVES: DESIGN CHALLENGES AND CHOICES

One of the significant challenges for any quartz alternative is frequency drift over temperature. The operating frequency range for XO typically varies from tens of kilohertz to tens of megahertz, while exhibiting better than ±25 ppm frequency drift over temperature without any electrical compensation. For high-precision applications like cellular systems (with <±5 ppm specifications), XOs are also electrically compensated. In contrast, applications like USB (500 ppm), S-ATA (350 ppm), and low datarate wireless links can tolerate much higher frequency drift over a given temperature range.

Fig. 2 shows the measured frequency drift over temperature for a 45-MHz Pierce oscillator using an inexpensive CTS AT-cut 45-MHz crystal resonator [2], employed...
as a frequency reference for one of our low power Medical Implant Communications Service (MICS) transmitter prototypes [3]. The specified frequency stability tolerance for −20 to 70°C for the crystal resonator used is ±50 ppm [2], which conforms to MICS transmitter requirements. The measured frequency drift over the 0 to 100°C temperature range is less than 50 ppm. The choice of temperature range is dictated by our test setup limitations. In this work, we attempt to achieve a similar level of stability without quartz.

We first compare the frequency drift over temperature of various uncompensated integrated oscillators. Fig. 3 shows the measured frequency drift over temperature for a standard on-chip LC-tuned oscillator [4], a native FBAR-tuned oscillator, a temperature compensated ZDR FBAR-tuned oscillator, and simulated results for an on-chip ring oscillator (RO). The frequency drift over the 0 to 100°C temperature range for a ZDR FBAR-tuned oscillator is around 100 ppm, as compared with approximately 30000 ppm (RO), 10000 ppm (LC VCO), and 3000 ppm (FBAR VCO). These measured results show that the design complexity for further electrically compensating a temperature compensated ZDR FBAR-tuned frequency reference is much less stringent than LC- or ring-oscillators, although it has been shown that the frequency drift over temperature for an LC-oscillator can be further reduced [5]. In this work, we demonstrate the combination of compensated resonators and on-chip temperature calibration circuitry for reducing frequency drift to <20 ppm.

Presently, there are primarily two commercially available quartz alternative technologies that target electronic systems with relaxed specifications:

1) All-CMOS LC Oscillators: This alternative uses an LC-tuned oscillator in a silicon CMOS process operating at high frequency, which is subsequently divided down below 100 MHz for clock applications [5]. Electrical compensation is used to cancel process, voltage, and temperature (PVT) variations of the LC oscillator.

2) Silicon Microelectromechanical Systems (MEMS) Oscillators: This alternative typically uses a module comprising a silicon MEMS oscillator operating at low frequency (generally in the kilohertz range) and a fractional phase locked loop (PLL) to multiply and obtain a programmable clock in the megahertz range.

Reference [6] provides a comparative analysis for MEMS frequency reference versus quartz devices. Although MEMS frequency references can achieve ±20 ppm frequency stability over temperature, they suffer from a power/phase noise trade-offs because of the PLLs and are not suitable for low-power wireless applications. Electrically compensated LC oscillators have shown <50 ppm [7], [8] residual frequency error over temperature, but they still do not meet frequency stability tolerance requirements over temperature for low-power wireless systems like Bluetooth, WLAN, etc. This work explores another possible low-power, low-form-factor quartz alternative: utilizing an FBAR-tuned oscillator for frequency reference generation. Native FBAR oscillators have demonstrated...
superior power/phase-noise performance compared with integrated CMOS LC oscillators [9], [10]. However, they show approximately −30 ppm/°C temperature dependency. As mentioned earlier, temperature compensated ZDR FBAR oscillators have recently shown immense improvement in reducing the frequency drift over temperature (approx. 150 ppm across 100°C), while still maintaining good power/phase-noise characteristics [11]. Without any electrical compensation, ZDR FBAR oscillators already provide performance sufficient for use as a clock in electronic systems with relaxed specifications. In this paper, we present a technique to further electrically compensate our FBAR-tuned CMOS oscillator to minimize frequency drift over temperature.

A comparative study of measured Q and the coupling coefficient \( k^2 \) for several families of mechanical resonators is presented in [12]. The resonator families included MEMS resonators, Lamb wave resonators, SAW resonators, AlN and ZnO SMR-BAW resonators, and FBAR resonators. The relative figure-of-merits (FOMs) are discussed, including unloaded Q, the f-Q product, \( k^2 \) and the \( k^2\text{-Q} \) product. The f-Q product is an important parameter to determine resonator feasibility for usage in clock applications. The f-Q product allows one to compare resonator performance irrespective of their frequency. The Avago compensated FBAR resonators have an f-Q product of \( 2 \times 10^{12} \) Hz [11], which is comparable to uncompensated MEMS and Lamb wave resonators. Uncompensated FBAR resonators demonstrate an f-Q product of \( 8 \times 10^{12} \) Hz. Thus, FBARs demonstrate an f-Q product approaching that of quartz in a batch fabricated process, allowing the possibility of inexpensive quartz replacement if frequency stability, aging, phase noise/jitter, and power consumption specifications can be met.

III. FBAR AS A TUNING ELEMENT

Fig. 4(a) shows cross-section of an FBAR. The Modified Butterworth-Van Dyke model (MBVD) shown in Fig. 3 is used to model resonance (series) and anti-resonance (parallel) FBAR behavior. \( C_0 \) represents the parallel plate capacitance of the FBAR resonator [13]. The oscillation frequency of an oscillator operating at the parallel resonance is given by [9]

\[
f_{\text{osc}} = f_s \sqrt{1 + \frac{C_m}{C_T}},
\]

where \( f_s \) is the series resonant frequency of an FBAR resonator and is modeled by \( L_m \) and \( C_m \), and \( C_T \) is the total capacitance accounting for \( C_0 \) and any capacitive loading from CMOS circuitry and tuning capacitor, with \( R_m, R_s, \) and \( R_0 \) representing resonator losses.

A free-standing membrane containing a piezoelectric material, AlN, is sandwiched between two molybdenum electrodes [14]. Energy exchange between the mechanical and electrical domains leads to a high-Q resonant behavior. Very little acoustic power is dissipated in the membrane motion at resonance because of high acoustic isolation provided by an air interface on both sides of the resonator. Fig. 5 shows the measured Q of the FBAR as extracted by the Bode method described in [12]. For an FBAR, as well as many other piezoelectric resonator devices, the Q is a function of frequency. Fig. 5 has two markers, one at the series resonance of the device \( (f_s = 1.500 \text{ GHz}, Q \sim 1573) \) and at the anti-resonance or parallel resonance of the device \( (f_p = 1.523 \text{ GHz}, Q \sim 742) \). The Q is a function of frequency for these devices because at the series resonance, \( f_s \), the device is practically a short and the Q is dependent on the residual acoustic loss plus the ohmic losses of the traces. At \( f_p \), the small amount of ohmic losses in the traces pales compared with the high resistance of the resonator \( R_p \sim 2000 \text{ to } 6000 \Omega \). Here,
the loss is dominated by the residual acoustic losses plus any residual energy loss leaking out at the edges of the resonators.

An unloaded Q greater than 1500 is typical for ZDR FBARs fabricated in the 0.5 to 7.5 GHz frequency range. However, unlike an on-chip inductor, the extremely high Q of an FBAR resonator does not directly translate into a correspondingly higher value of parallel resistance. Therefore, the CMOS circuit impedance need not be extremely large to avoid reducing the Q of the resonator. A measured impedance versus frequency profile of an FBAR resonator, as well as for an on-chip LC tank (Q = 10), is shown in Fig. 6. The high quality factor behavior of an FBAR resonator is apparent in the measurement as compared with the on-chip LC tank.

The FBAR resonator impedance is real with a value less than few ohms at its series resonance, whereas at the parallel resonance the impedance is real with a value greater than 1 kΩ. The LC-tank exhibits one low-Q resonance with a parallel resistance $R_p$ close to 1 kΩ. Unlike an on-chip LC tank, which is inductive at low frequencies and allows dc current flow, an FBAR resonator is capacitive at low frequencies and exhibits a high impedance. From a designer’s perspective, FBAR resonators are an attractive option for use as a tuning element in low-power frequency reference oscillators with low phase noise because FBAR resonators have a much higher quality factor than any other on-chip resonant structure.

A native FBAR shows a temperature dependence of $-30$ ppm/°C. The negative temperature coefficient of AlN (the piezoelectric) and Mo (the electrodes) dominates the FBAR resonance drift with temperature. As demonstrated in [11], the negative dependence can be canceled by depositing a thin layer of oxide, a material with positive temperature coefficient. After mechanical compensation, these ZDR FBARs show approximately 150 ppm frequency drift over a 100°C temperature range. Fig. 7 shows a histogram of the spread in frequency after final trim. The measured standard deviation is 100 ppm for this wafer.

The distribution of the series resonance across the wafer is also plotted in Fig. 7. The wafer contains approximately 128,000 die per 150 mm diameter wafer. The trimming process used here is a modification to the standard manufacturing technique used for FBAR filters and duplexers, which typically target a 500 ppm standard deviation.

Fig. 8(a) is a wafer plot showing the measured TCF for a 6-inch wafer. The number of sampled die for this figure is on the order of several thousand points. For achieving a TOT of 65 to 70°C, we have determined that the measured TCF should be around 0.8 ppm/°C. Fig. 8(b) shows the temperature response of the series resonance, $f_s$, of 400 die over 18 different temperatures. The series resonance frequency has a measured $\beta$ of approximately $-17$ ppb/°C$^2$. The parallel resonance frequency, $f_p$, has a measured $\beta$ of approximately $-30$ ppb/°C$^2$. Although $f_p$ is the resonance of interest for our oscillator design, we monitor $f_s$ on wafer due to the relative measurement robustness in determining frequency.

IV. FBAR/CMOS FREQUENCY REFERENCE

The goal of this work is to integrate a system that removes the residual frequency variation caused by temperature changes in ZDR FBAR-based oscillators. The block-level diagram of our FBAR-based frequency reference is shown in Fig. 9. Similar to frequency stabilization techniques implemented on a recently published quartz crystal reference [15], we can address temperature instability using on-chip real-time temperature calibration of an FBAR-tuned oscillator. Temperature compensation for a BAW-tuned Colpitts 2.5-GHz oscillator using a switched capacitor varactor is presented in [16], but the calibration is not performed on-chip in real time. Our on-chip temperature calibration is performed as a three-step process:

1) **Sensing and amplifying temperature variations:** This is accomplished by a combination of an on-chip proportional to absolute temperature (PTAT) temperature sensor and a precision switched capacitor amplifier.

2) **Digitizing temperature variations:** A 7-bit low-power successive approximation register (SAR) ADC digi-
izes the output of an on-chip switched-capacitor absolute temperature sensor. This digitized temperature reading addresses an integrated programmable 1024-bit look-up table (LUT).

3) Fine frequency tuning using a lookup table (LUT): A pre-stored temperature compensation profile is stored in an on-chip SRAM. The ADC addresses the LUT as the temperature changes, resulting in an appropriate frequency correction capacitor setting. The contents of the LUT controls an 8-bit binary weighted capacitor array with a corresponding frequency LSB step size of 0.7 ppm, allowing completely self-contained temperature compensation.

A. Sub-Milliwatt FBAR Oscillator Design

One can divide oscillator classes into 2 families: series oscillators and parallel oscillators. The latter, an oscillator that resonates at or near the parallel resonance frequency and with additional capacitance added by a varactor (or switches), will move counter clockwise toward $f_s$ on a Smith chart. The oscillation frequency lowers with the additional capacitance. A series oscillator operates near $f_s$ and the varactor and/or switches are used to pull the operating point away from $f_s$. Many oscillator topologies including cross-coupled, Pierce, and Colpitts, etc. operate in the parallel oscillation mode. The Pierce oscillator topology is known for its frequency stability. The capacitor loading for the resonator in Pierce topology is grounded on one side, making the switched-capacitor design simple and less sensitive to bias current variations. A single-ended design is chosen over our previous differential design in [10] to improve the power/phase noise performance. It is important to maintain monotonicity of the capacitor trimming bank to allow accurate frequency variation cancellation over temperature. The frequency sensitivity to capacitor change for the FBAR-tuned oscillator is given by

$$\frac{\delta f_{osc}}{\delta C_T} = f_s \text{series} \frac{C_x}{2C_T^2}.$$  

providing a roughly linear frequency variation for small values of capacitor pulling.

To achieve good linearity for frequency tuning, this design uses discrete switching of pMOS capacitors to obtain sub-ppm frequency accuracy. The aspect ratio of the unit pMOS capacitor used in this design is (0.72/0.4) µm, which results in <1 fF effective change in capacitance seen by the oscillator between on- and off-state. The Q of such a small capacitor in CMOS technology does not degrade the FBAR oscillator performance. The oscillator and capacitor bank design in this work has been optimized to achieve sub-ppm frequency LSB step across PVT variations. The total tuning range using an 8-bit binary capacitor bank is approximately 200 ppm.

B. Temperature Readout Circuitry

The temperature readout circuitry comprises an analog PTAT sensor, a switched capacitor analog amplifier, and
a 7-bit SAR ADC. The design of the temperature sensor is based on switching ratioed currents through a single diode [17]. This approach eliminates area-matching constraints for the temperature sensing diode, reducing noise in the temperature readout. As a continuous readout is not required, a switched capacitor amplifier is used to amplify the analog readout voltage before sampling and digitizing with the ADC. A SAR ADC architecture is chosen for its ultra-low power operation capability. The temperature readout circuitry, as well as 1024-bit LUT, uses a sub-kilohertz system clock. This clock can be derived from the FBAR-tuned oscillator.

Fig. 10 shows details for logic interface between the SAR ADC, LUT, and oscillator capacitor array. During one cycle of temperature compensation, the on-chip switched-capacitor temperature sensor delivers an analog signal which corresponds to the real-time temperature. It also generates a digital ready-to-convert signal for the 7-bit SAR ADC after the analog output settles. As shown in the timing diagram in Fig. 11, the ADC then digitizes the analog output from the temperature sensor. The 128-word, 1024-bit SRAM LUT is addressed by the 7-bit SAR ADC output. Upon receiving a handshaking signal from the SAR ADC after the 7-bit digital outputs are ready, the LUT updates the 8-bit binary output content. The handshaking signal from ADC acts as an Enable signal to the SRAM block. The updated 8-bit binary SRAM output is then used to control the capacitor array of the FBAR-tuned oscillator to correct the frequency drift caused by temperature variations. Each SRAM memory cell is constructed from a pair of cross-coupled inverters (a 6-T cell). The SRAM is addressed only once during each compensation cycle.

V. MEASUREMENT RESULTS

The system was implemented in a 0.35 μm CMOS process with die size of 0.79 mm × 1.72 mm. Because this prototype aims to demonstrate electrical temperature compensation for FBAR-based oscillators, the silicon area is dominated by the number of bondpads used for testability. The FBAR is wirebonded directly to the CMOS chip. The micrograph of the assembled system is shown Fig. 12. The measurement setup for this prototype is shown in Fig. 13. The chip operates in two modes. In the calibration mode [Fig. 13(a)], the temperature profile of the free-running FBAR oscillator is measured. Using this information, software processing in MATLAB generates a complementary calibration code for real-time temperature correction. Calibration code is the 8-bit binary code that the capacitor bank requires for a given temperature to correct the frequency drift of the FBAR oscillator. After the calibration code is programmed into an on-chip 1024-bit LUT, the measurement is run in free-running mode [Fig. 13(b)].

Fig. 14 shows the measured output of the FBAR oscillator for 3 different samples, with compensation on and compensation off. When the compensation circuitry is turned off, the oscillator inherits the temperature stability of the FBAR resonator, resulting in a worst case frequency drift of approximately 150 ppm measured over a 100°C temperature range. In this work, the limited temperature range of 0 to 100°C is dictated by our measurement test setup capability. The frequency drift is reduced to <±10 ppm post-compensation without any averaging in the measurement. In a separate experiment, the data points were collected continuously for a transient temperature ramp rate of 5°C/minute and the frequency error remains below 20 ppm post-compensation, as shown in Fig. 15. The frequency error can be further reduced by averaging the temperature readout in the digital domain. A 10-point post-calibration averaging in software
allows reducing the frequency error below $\pm 5$ ppm in Fig. 15. The performance summary for the FBAR/CMOS frequency reference is tabulated in Table I.

The FBAR oscillator consumes 510 $\mu$A and has a measured phase noise of $-133$ dBC/Hz at a 100 kHz offset with 2 V supply voltage as shown in Fig. 16. The integrated phase jitter for 10 kHz to 10 MHz frequency range is 0.04 ps rms. It should be noted that Fig. 16 shows the measured phase noise for the FBAR oscillator, with compensation loop off at room temperature and no active switching of discrete capacitors. The measured phase noise variation at 100 kHz frequency offset versus oscillator current consumption is plotted in Fig. 17, and shows better than $-130$ dBC/Hz

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating frequency</td>
<td>1.5 GHz</td>
</tr>
<tr>
<td>Silicon die area</td>
<td>0.79 mm x 1.72 mm</td>
</tr>
<tr>
<td>Measured temperature range</td>
<td>0 to 100°C</td>
</tr>
<tr>
<td>Frequency drift (ppm) vs. temperature</td>
<td>$\pm 10$ (Compensation ON), $\pm 50$ (Compensation OFF)</td>
</tr>
<tr>
<td>Phase noise (dBC/Hz) at 100 kHz offset</td>
<td>$-133$</td>
</tr>
<tr>
<td>Expected phase noise (dBC/Hz) at 1 kHz offset from divided 13 MHz carrier</td>
<td>$-127$</td>
</tr>
<tr>
<td>Current consumption ($\mu$A) at 2 V power supply</td>
<td>Oscillator 510 PTAT + ADC + LUT$^1$ 5</td>
</tr>
</tbody>
</table>

$^1$PTAT = proportional to absolute temperature sensor; ADC = analog-to-digital convertor; LUT = look up table.
Hz at 100 kHz offset for 400 µA or more oscillator bias current. Theoretically, for a divided frequency output of 13 MHz, the expected phase noise is −127 dBc/Hz at 1 kHz offset and the phase jitter for a 10 kHz to 10 MHz frequency range is <1 ps rms. The on-chip temperature calibration circuitry consumes less than 5 µA.

The digital switching of capacitors for temperature compensation results in frequency discontinuities and spurs. Fig. 18 shows the measured spectra using an Agilent PSA E4446A (Agilent Technologies, Santa Clara, CA), with and without compensation circuitry turned on. When the temperature compensation circuitry is on, we enable MAX HOLD for 30 s to capture the 200 kHz frequency span close-in spectrum at room temperature, with compensation loop frequency of 200 Hz. As seen in the Fig. 18, although the frequency stability is <10 ppm, the close-in noise floor is raised because of the frequency discontinuities and spurs. The sensitivity to these frequency discontinuities or phase jumps is very application specific. For example, cellular systems using phase modulation techniques cannot tolerate an increase in bit error rate (BER) caused by these phase jumps. In contrast, low-power applications like ISM transceivers employing FSK modulation are insensitive to small frequency discontinuities relative to their symbol spacing, and a <1 ppm frequency jump will not affect their BER performance. One approach to avoid frequency discontinuities is through the use of an analog capacitor and generating a programmable complementary frequency drift curve for temperature compensation as shown in [18]. Similarly, in a digitally switched capacitor compensation scheme, the transition rate of bit switching can be reduced drastically to shape the frequency transitions.

VI. Conclusion

ZDR FBAR-tuned oscillators show potential for quartz replacement in applications tolerating <±50 ppm frequency drift over a 100°C temperature range. Further electrical compensation is needed for a quartz-free miniaturized ZDR FBAR frequency reference for wireless applications where the maximum tolerable frequency drift is ±10 ppm over temperature. This work demonstrates a low-power 1.5 GHz FBAR/CMOS frequency reference with low-temperature sensitivity for wireless applications. Divided frequencies in the range of 10 to 150 MHz can be used for quartz replacement in miniaturized electronic systems that do not demand stringent frequency stability and are insensitive to small frequency discontinuities.
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REFERENCES


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Rich Ruby obtained his B.S., M.S., and Ph.D. degrees at the University of California, Berkeley, CA, in 1977, 1981, and 1984, respectively. His Ph.D. work was in superconductivity. After his graduate work, he joined HP Labs (later to become Agilent Labs, and now Avago Technologies) working on superconductivity, E-beam lithography, X-ray lithography, and packaging. In 1993, he started work on free standing bulk acoustic wave resonator devices (FBAR) and has stayed with that technology since. He has made many contributions to the commercialization of FBAR filters and duplexers. He was made an Agilent Fellow in 2002 and holds that title as well as director of technology at Avago. Rich Ruby was made an IEEE Fellow in 2009. He was also awarded the Barney Oliver Prize and the Bill Hewlett Award for his work on FBAR technology. Rich holds more than 50 patents in the area of FBAR devices and has given numerous invited papers. Over the last decade, the FBARs have won several industrial awards for innovation.
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