An 8x8 Row-Column Summing Readout Electronics for Preclinical Positron Emission Tomography Scanners

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Abstract–**This work presents a row/column summing readout electronics for an 8x8 silicon photomultiplier array. The summation circuit greatly reduces the number of electronic channels, which is desirable for pursuing higher resolution positron emission tomography scanners. By using a degenerated common source topology in the summation circuit, more fan-in is possible and therefore a greater reduction in the number of electronic channels can be achieved. The timing signal is retrieved from a common anode, which allows the use of a single fast-sampling analog to digital converter (ADC) for the timing channel and slower, lower power ADCs for the 64 spatial channels. Preliminary results of one row summation of the 8x8 readout electronics exhibited FWHM energy resolution of 17.8% and 18.3% with and without multiplexing, respectively. The measured timing resolution is 2.9ns FWHM.**

I. Introduction

With the development and miniaturization of modern silicon photomultipliers(SiPMs), smaller detector modules becomes possible to achieve high resolution positron emission tomography (PET) scanners. However, as the detector size is reduced to achieve the best spatial resolution, the required number of readout channels scales accordingly. This complicates the interconnection between detector modules and post processing electronics, and raises the capability requirements on the back end electronics. At the University of Washington we are building high resolution pre-clinical PET scanners based on our experience with the micro crystal element detector mouse scanner (MiCES) electronics concepts [1,2]. In this work, we use a row-column summing scheme which can effectively reduce the number of electronic channels from N^2 to 2N, for an N by N array. By performing the summation in the front-end electronics, the number of analog to digital converters, as well as the number of electronic channels to the digital processing units, can be greatly reduced with little degradation in energy resolution. In addition, the timing signal is obtained from the single common anode signal. This allows the use of a very fast ADC for the timing channel and slower, lower power consuming amplifiers and ADCs for the positioning channels. These features are critical in pursuing higher resolution PET scanners with fine-pitch photosensor arrays.

Based on the concepts above, a prototype row-column summing electronics is developed to evaluate the effects of row-column summing on an 8x8 SiPM array and common anode timing signal pick-off. This circuit design is being investigated to support the depth of interaction micro crystal element (dMiCE) detector being developed at the University of Washington [3,4]. Successful results will lead to the development of an efficient application specific integrated circuit (ASIC) based upon this architecture.

II. Detectors and Crystals

The summing electronics is currently designed to interface with a prototype 8x8 SiPM array (MAPD-3N, Zecotek Photonics Inc.), as shown in Fig. 1(a) and 1(b). It is comprised of an 8x8 array of individual photodetection elements, each with its own cathode output. The bias voltage of the detector is around 88V to 89V. The center-to-center spacing between elements is 3.6mm, while the whole detector array measures 3.3cm, including the ceramic package. Fig. 1(a) shows its connector on the back side of the detector array. While all the cathodes of the 64 elements have their own connector output, the anodes are wired together as the common anode channel. This feature facilitates reading out signals from the common anode, which will be described in detail later. Fig. 1(c) shows the 8x8 lutetium-based scintillator crystal array (LFS-3, Zecotek) that we will use with the detector array in the future. Each element of the crystal array is optically isolated in diffuse reflecting material, and measures 3.5mm by 3.5mm by 20mm. The small form factors of these detector array and crystal array allow building a compact detector module to realize high resolution PET scanners.

III. Architecture and Circuit Design

While the electronics presented in this work is based on discrete circuit components, the purpose is to study the effects of row-column summing and the common anode signal pick-off. Our goal is to map the circuit architecture to a future ASIC to achieve the miniaturization of the whole detector module. Fig. 2(a) shows the architecture of our proposed detector module. For each detector module in Fig. 2(b), an ASIC reads out the signals from an 8x8 detector array,

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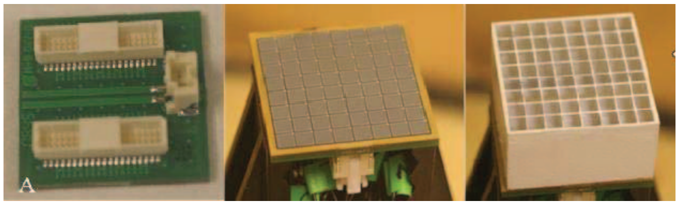
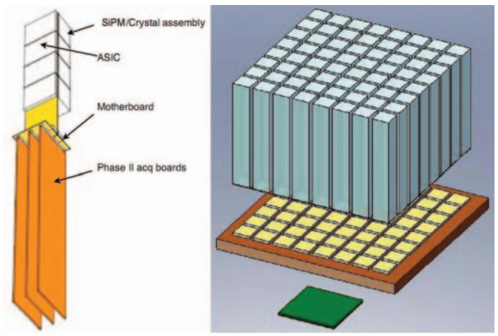


(a) (b) (c)

Fig. 1(a) Connectors of the 8x8 SiPM array (b) SiPM elements (c) 8x8 LFS crystal array



(a) (b)

Fig. 2 (a) Architecture of the proposed detector module (b) Detector assembly

including 64 cathode signals and one common anode signal. The 64 cathode signals are row-column-summed into 16 summed signals before sending to the acquisition board. This board contains the ADCs for digitizing the signals from the ASIC, the Firewire transceiver IC, various communication and control lines, and the field programmable gate array (FPGA) with additional external memories[2].

The block diagram of the prototype readout electronics is shown in Fig. 3. The board provides the biasing circuitry to the SiPM array; detects and amplifies the signals from the array; and performs row/column summation of the 64 cathode signals. The biasing circuits on the board biases the 8x8 SiPM array from both the common anode side and the individual cathode sides. Thus, the signal at the anode side is effectively a summed version of all the 64 channels. This common anode signal is amplified by high-bandwidth operational amplifier chains to retrieve the timing information.

The signals on the cathode side are amplified by off-the-shelf variable gain amplifier (VGA) ICs, whose gain can be individually set with serial-peripheral-interface (SPI) controlled digital potentiometers. For depth of interaction (DOI) measurements using light sharing between neighbor pixels, a gain adjustment mechanism is needed before the summation circuitry due to the intrinsic gain variation between each MAPD detector element and the associated scintillator crystal. The VGAs provide gain normalization to compensate mismatches between detector elements and scintillator crystals.

A summing circuitry performs row-column summing on the amplified cathode signals. The subsequent output buffers convert each of the single-ended, summed signals into differential pairs for better electromagnetic interference immunity, and drives the interconnect cables which connects to measurement instruments or other post processing electronics.

To simultaneously pick up signals from both the common anode and the individual cathodes, the SiPM array is biased with resistors on either side of the device (Fig. 4.). Coupling capacitors are used to isolate the DC voltage. Since the timing resolution is inversely related to the slope of the signal, high-bandwidth electronics is usually needed for obtaining good timing resolution. In contrast to [5], where signals are sensed only on one side, our approach significantly reduces the number of discriminator circuits and alleviates the bandwidth requirement for the electronics in the individual channels, resulting in a more cost-effective, more compact front-end circuit. More importantly, power consumption can also be greatly reduced. This is crucial for compact PET scanner detector modules due to stringent power and heat dissipation requirements, as the performance of SiPMs are strongly dependent on the junction temperature [6].

The individual cathode channels are used for obtaining spatial information. Thanks to the orthogonality of the row/column summation scheme, the readout signals can be used as the coordinate of the original signal in most situations. This information can be used to determine the energy window based on the corresponding photodetector characteristic.

Several signal multiplexing techniques have been proposed to reduce the number of electronic channels. Resistive charge division is easy, compact, and inexpensive to implement, but the crosstalk between different channels through the resistive network may degrade the system performance [7]. In this case, a high threshold setting may be necessary in the subsequent discriminator circuits to exclude invalid events due to cross-talk. However, for the light sharing techniques for DOI measurements under research in our lab, where multiple

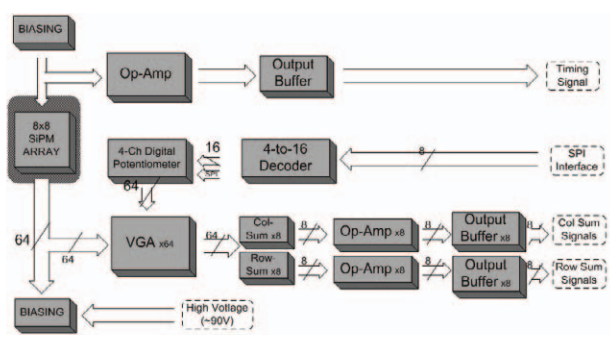


Fig. 3. Block Diagram of the readout electronics.

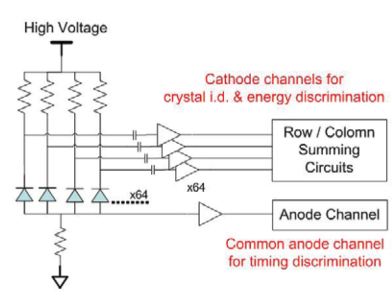


Fig. 4. Biasing circuit for simultaneous signals pick-off on the common anode and individual cathodes

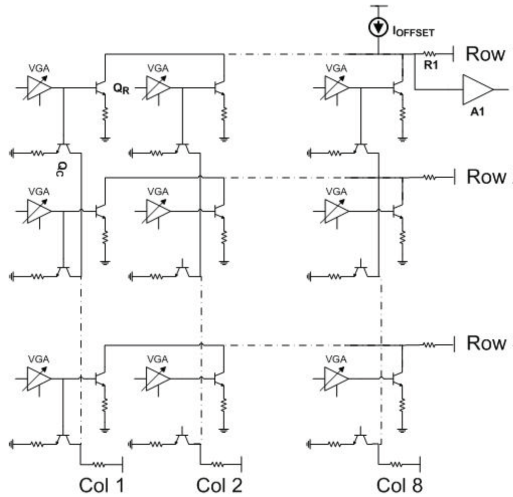


Fig. 5 Row/column summation topology

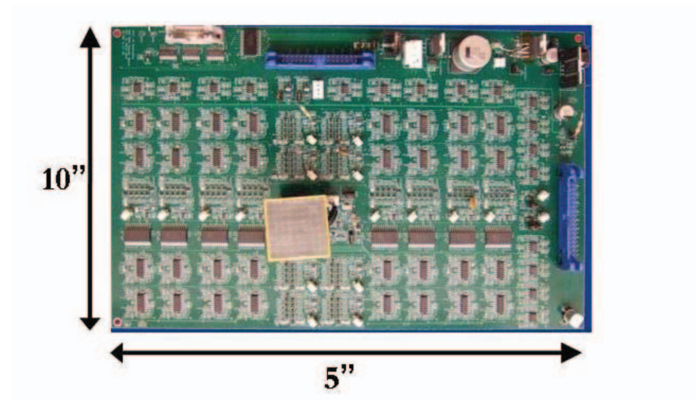


Fig. 6 Board photo

signals must be read out at the same time, the cross-talk between channels can potentially degrade the signal quality. Other techniques like capacitive multiplexing and analog signal multiplexing are limited in fan-out numbers and therefore not suitable for applications where large number of reduction is needed [8,9]. A multiplexer design in [10] demonstrated superior noise properties to a resistive network. However, this technique does not apply to applications where multiple signals must be read out simultaneously, which is required for certain DOI measurement techniques [3].

Motivated by the above concerns, a new summation scheme for row/column summation in PET scanners is proposed. The summation is achieved with a degenerated common source topology (Fig. 5). In this example, each of the 64 variable gain amplifiers (VGA) drives the bases of two NPN transistors (Q_R and Q_C), one for row summation and one for column summation. The NPN transistor with a source resistor approximates a linear voltage-to-current converter. The 8 currents of the same column or row are wire-summed across the array. A current source, I_{OFFSET}, removes the DC current from the common collector node. The signal current flows through a load resistor R_1 and establishes a voltage which is amplified by op-amp A_1. Since the signal from the previous stage is buffered by a transistor, which has very large input impedance, the leakage current path as in [7] is eliminated and crosstalk introduced by the summing network is therefore greatly reduced. Additionally, for most of the cases in which multiple simultaneous signals arrive at the same time, the original signals could still be retrieved by post-analyzing the 16 row/column signals.

IV. Results

A photo of the developed prototype board is shown in Fig. 6, together with an 8x8 SiPM array located in the center region of the board. The board is made of 8 layer FR4 printed circuit board and measures 5 inches by 10 inches.

To evaluate the effect of row-column summing, preliminary experiments on energy resolution are performed with the setup shown in Fig. 7. In this experiment, a 511 keV Ge-68 radiation source is used. A 1x8 LFS crystal array individually wrapped in Teflon is mounted on the row of interest. Its corresponding row-sum signal is sent to spectroscopy amplifier for pulse shaping and then multi-channel analyzer (MCA) for digitalization. To measure the energy spectrum of one particular detector element, its corresponding orthogonal column-sum channels is sent to a constant fraction discriminator at the same time as a trigger to the MCA. In the example of Fig. 7, column-sum channel 5 is used for discrimination to measure the energy spectrum of detector element E5. Therefore, only pulses that are simultaneously probed in the row and column channel are counted in the energy spectrum.

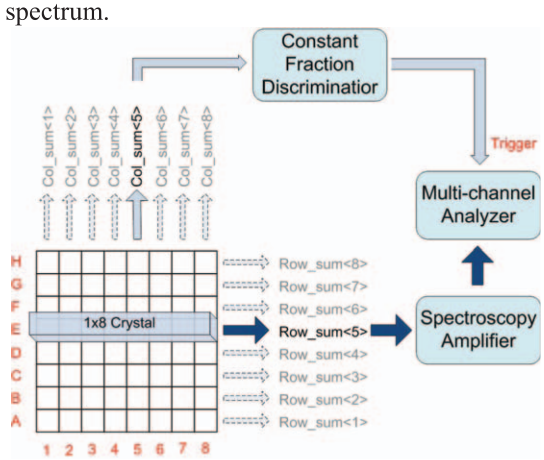


Fig. 7 Experiment setup for energy resolution measurement

With a 1x8 crystal, the measured FWHM energy resolution from the summed channel is 17.78% before multiplexing, where only one of the eight VGAs in the same row is turned on with nominal gain setting. All the other 7 VGAs in the same row are set to minimum gain, which is 23dB lower then the nominal value. After multiplexing, where all of the eight VGAs in the same row are set to nominal gain, the measured energy resolution is 18.28%. The degradation in energy resolution is credited to the increased electronic noise, SiPM detector noise, and crystal activity associated with the summed channels. To evaluate the influence of summing on energy resolution excluding crystal activity, another experiment is performed with only one single crystal mounted on the element of interest. The measured energy resolution before and after multiplexing is 12.14% and 13.75%, respectively. The measured energy spectra are shown in Fig. 8. While we are still sorting out the cause of the energy resolution differences with one single crystal and with 1x8 crystal array, it is worth noting that in both cases, the degradation in energy resolution before and after multiplexing is less then 1.7%. These experiments show promising results for the proposed row-column summing technique.

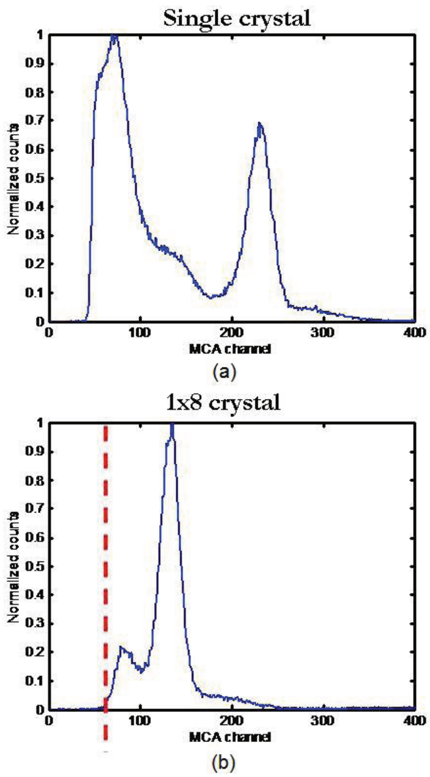


Fig. 8 Energy spectra from cathode channels (a) with single crystal (b) with 1x8 crystal array

To evaluate the cross-talk between channels, a single crystal is mounted on one of the 8x8 detector array. Its corresponding row-sum and column-sum signal, as well as a neighbor row-sum signal is probed on oscilloscope. As shown in Fig. 9, there are simultaneous events in the corresponding row and column sum channels while no event is detected in the neighbor channel. Therefore, it can be concluded there is no significant cross-talk between channels.

The experiment setup used for measuring timing resolution is shown in Fig. 10. A single SiPM detector with a single LFS crystal is used as a coincidence detector, while another single crystal is mounted on one element of the detector array. The common anode signal from the detector array is amplified by the electronics on the prototype board before being sent to timing measurement instruments in Fig. 10. The measured FWHM timing resolution from the common anode channel is 2.91ns. Measurement result is shown in Fig. 11. As the timing performance is strongly dependent on the length of leads and traces, the timing resolution obtained with the prototype board is not optimized.

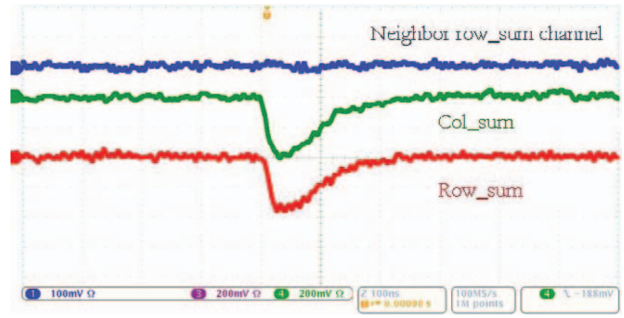


Fig. 9 Cross-talk experiment

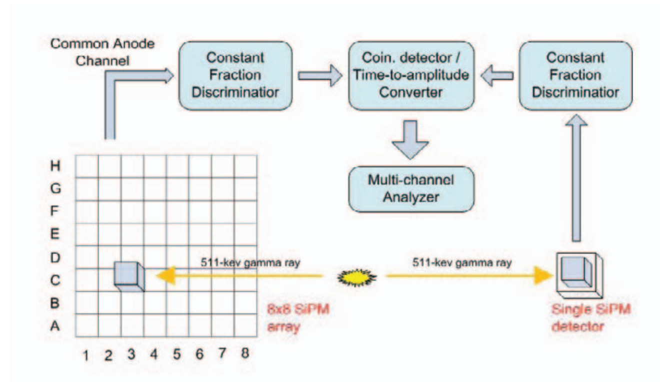


Fig. 10 Experiment setup for timing resolution measurement

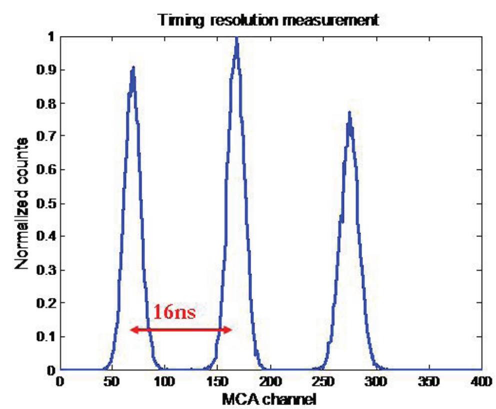


Fig. 11. Timing resolution measurement result

We believe mapping the circuit architecture into an ASIC will provide significant improvement in the timing performance. Nevertheless, it is good enough for most non-time of flight applications.

V. Conclusion

A proof-of-concept 8x8 SiPM readout electronics is presented. The board reads out the common anode signal and the 64 cathode signals from the detector array. Common anode signal is used as a timing signal. The measured timing resolution is 2.91ns. The 64 cathode signals are row-column-summed into 16 signals. Experimental results of energy resolution so far are summarized in Table I. The energy resolution with different number of multiplexing is measured by setting corresponding number of VGAs to minimum gain (23dB lower than normal value). In both the single crystal experiment and the 1x8 crystal array experiment, the energy resolution degradation is less then 1.7%.

In the future we will continue to measure and analyze the data with the 8x8 crystal array and to optimize the readout electronics for better performance. We will also integrate this readout electronics to the acquisition board under development in our lab [11,12].

TABLE I. SUMMARY OF CATHODE CHANNEL ENERGY RESOLUTION

Crystal	Channels Multiplexed	Energy resolution
Single crystal	1	12.14%
	4	12.94%
	8	13.75%
1x8 crystal array	1	17.78%
	8	18.28%

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