A 2.6 GHz, 25 fs jitter, Differential Chip Scale Oscillator that is <1 mm^2 in area and 0.25mm tall

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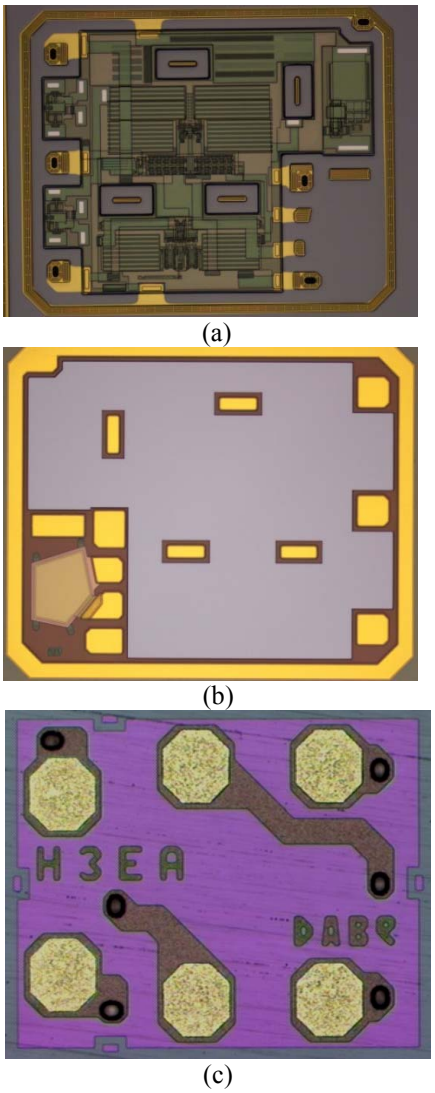
Abstract — **We demonstrate a 2.6 GHz chip-scale oscillator that measured phase noise better than -150 dBc/Hz at 1 MHz offset and integrated jitter of just 25 fs. The part was designed with differential out and drives a 100 Ohm differential load with a mean voltage swing of 100 to 200 mV. The phase noise at 10 kHz offset is -110 dBc/Hz. The device runs at 3.3V and Idd is just over 9mA (including buffer). Another variant is designed to have an on-chip varactor allowing tuning of 615 ppm/V over the targeted 0.5 to 1.8 V tuning range. Here, the integrated jitter degrades by 2X at 0 V Vtune and we measured 85 fs jitter at 1.5 V Vtune. Still, the integrated jitter was well below 100 fs. The all-silicon packaged part is designed to directly solder down onto a PCB. There are no bond wires used in the assembly of this device. The height of the soldered part is under 0.25 mm, and the area of the die is less than 1 mm^2. The oscillator uses a Zero Drift Resonator (ZDR) FBAR and we see about +/- 100 ppm temperature drift from -40C to +110ºC. The design uses a cross-coupled architecture with the ZDR and is ac-coupled to a buffer amplifier.**

Index Terms **— FBAR, BAW, frequency reference, oscillator, quartz replacement**

I. Introduction

FBAR's high f*Q product makes it an appealing alternative to conventional low-jitter RF frequency synthesis methods. Our previous work demonstrated the potential value of an FBAR [1], a wafer scale hermetic package [2], a modified FBAR demonstrating temperature stability comparable to quartz (referred to as Zero Drift Resonators, or ZDR [3]), and a sub-mW oscillator using FBAR [4]. We have also demonstrated a technique for integrating active circuitry into the lid of the wafer-scale hermetic FBAR package while the FBAR resonator, ZDR, or filter resides on the base wafer [5]. Because process modification of the lid/IC wafer is minimal, this strategy is compatible with any IC technology. Other than imposing an area limitation on the circuit, no special circuit design rules are required.

Previously we used Pierce and Colpitts oscillators to demonstrate this FBAR – IC integrated hermetic package [5]. In this work, we propose a fully-differential oscillator that allows large signal swings and true balanced outputs to drive a 100 load. Unlike designs using LC-tuned VCOs, we use an FBAR-tuned oscillator to achieve extremely low jitter (25fs) at RF frequencies. The FBAR or ZDR wafers can be fabricated in a wide variety of frequencies. We have demonstrated 1.7 GHz, 2.6 GHz, and 3.4 GHz in this work.



(a)

(b)

(c)

Figure 1: Micrograph of disassembled hermetic oscillator package containing A) lid with integrated active circuitry; B) ZDR base wafer. C)The completed part with Cu/Ni/Au pads and dimensions of 1.07 mm by 0.89 mm

II. Process Overview

As described in detail earlier [5], wafer fabrication is based upon existing processes wherever possible. In the Avago microcap process, the ZDR is fabricated on one wafer while a second lid wafer contains through-wafer vias, pads, bonding structures, and a recessed cavity above the ZDR. Figure 1 is a micrograph of an opened package showing the ZDR die and the lid containing the active circuitry.

The circuits were implemented using Avago's HP25 silicon bipolar process. Prior to patterning the standard microcap lid structures, one additional etch step was used to remove the inter-layer dielectric in the field areas to expose the Si surface. The electronics require a highly-doped epitaxial Si layer (<5 -cm) that would short the through-wafer vias, but the epitaxial layer was removed between vias during the standard cavity recess etch used to form the microcap bonding structures. The lid Au metallization connects the circuitry to the ZDR after the wafers are joined together.

Figure 2 contains an SEM cross-section of a bonded die, in which the relative position of the ZDR and the lid circuitry are shown. To provide clearance for wafer bonding, the circuitry on the lid aligns with a corresponding depression in the ZDR wafer. Both wafers are high resistivity Si (>1500 -cm) to minimize parasitic coupling to the ZDR and crosstalk between the through-wafer vias. We have retained the Au-Au wafer bond that has been proven to provide a highly robust hermetic seal [6].

The completed chip-scale oscillator is shown in Figure 1(c), with final dimensions of 1.07 mm by 0.89 mm and a height of 0.25 mm. In this work, we have six external pads and two internal connections from the lid electronics to the ZDR resonator. The Cu/Ni/Au pads allow the part to be directly soldered down onto a PCB, eliminating the need for bond wires.

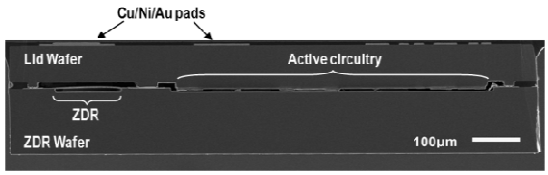


Figure 2: Cross-section SEM of FBAR/bipolar process showing full finished die.

III. Circuit Implementation

Figure 3 shows the fully-differential oscillator and buffer circuits that are integrated into the lid. All bias circuitry is integrated. Cross-coupled NPN transistors $N_{1,2}$ generate a negative resistance with an equivalent value of -2/gm. At resonance, this negative resistance cancels out the parallel resistance from the load tank circuit formed by the ZDR and the total capacitance at the oscillator output nodes. The output common-mode is first sensed through two resistors, level-shifted through replica transistor N_5, and then fed into the base of the foot transistors to form a negative-feedback stabilization loop. At low frequencies, the FBAR resonator is capacitive. The loop gain at low frequencies is therefore high, potentially allowing oscillation at undesired frequencies. To prevent parasitic modes of oscillation, we have inserted a capacitor C_1 at the emitters of $N_{1,2}$. At low frequencies, the capacitor acts as an open circuit. The loop gain is lowered as the transconductance of the cross-coupled pair is degenerated by $N_{3,4}$ [6]. At high frequencies, the capacitor acts as a short circuit. The cross-coupled pair exhibit high transconductance as their emitters see a virtual ground. As a result, a high loop gain ensures proper oscillation. The capacitance value is chosen to minimize loop gain at low frequencies and maximize loop gain at the frequency of interest. In another variant, varactors are added at the outputs to provide tuning capabilities.

The outputs of the oscillator are AC-coupled to the buffer, designed to drive a 100 differential output load. The buffer uses a modified emitter-follower topology, where the signal drives the follower transistors $N_{8,9}$ as well as the current source transistors $N_{10,11}$. This current-reuse technique effectively doubles the transconductance and gain of the buffer for the same current consumption. AC-coupling through $C_{4,5}$ separates the DC bias voltages for $N_{8,9}$ and $N_{10,11}$. High current in the buffer is required to drive 100 ; however, this reduces the base resistance at the input of the buffer. To avoid loading down the resonant tank, we insert a Darlington current buffer stage between the oscillator and the buffer. By scaling down the current in the $N_{6,7}$, we increase the base resistance and minimize de-Q-ing of the resonant tank.

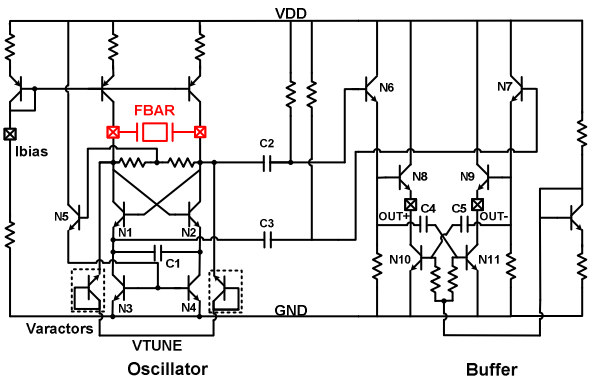


Figure 3: Schematic of the oscillator and buffer.

IV. EXPERIMENTAL RESULTS

The completed chip-scale oscillator is flip-chip bonded to a PCB. External components include a decoupling capacitor between power and ground, as well as DC-blocking capacitors at the two VCO outputs. For measurement purposes, a balun is also employed at the output for differential-to-single-ended conversion.

The total bias current from the oscillator core and the buffer increases from 7.5 to 12.5 mA, while the output power increases from -11 to -3.8 dBm when the supply varies from 2.75 to 4.25 V (Figure 4). The simulated oscillator current ranges from 1.2 mA to 2 mA as the supply increases from 2.75 to 4.25 V.

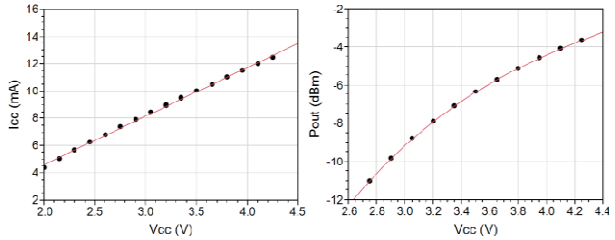


Figure 4: Measured oscillator current (left) and output power (right).

Relative to a conventional FBAR, the ZDR device removes the linear temperature drift around a fixed turn-over temperature (TOT), yielding a residual second order temperature dependence on the order of -15 to -30 ppb/˚C^2. The ZDR in these devices have a TOT of approximately 40˚C. Fig. 5(A) shows the frequency drift of the oscillator attached to a 2.6 GHz ZDR resonator when the temperature varies between -40 to 110˚C. To improve oscillator temperature stability to below 100ppm (over a 100˚C temperature range), we could include a feedback loop to measure temperature similar to the one described in [5]. Fig. 5 (B) shows the frequency change as a function of supply voltage. Approximately 250 ppm of frequency variation is observed over a ±10% change in the supply voltage (at 3.3V). Frequency sensitivity over a 2:1 change in load VSWR is on the order of 15 ppm.

For the oscillator, we experimented with two kinds of ZDR resonators: one with a high Rp (lower Q) acoustic stack and one with a lower Rp (higher Q) acoustic stack. The latter stack in the oscillator gave 3 to 8 dB better measured phase noise (1kHz to 1 MHz) and the measured jitter was 25 fs. However, the output power was approximately 6 dB lower.

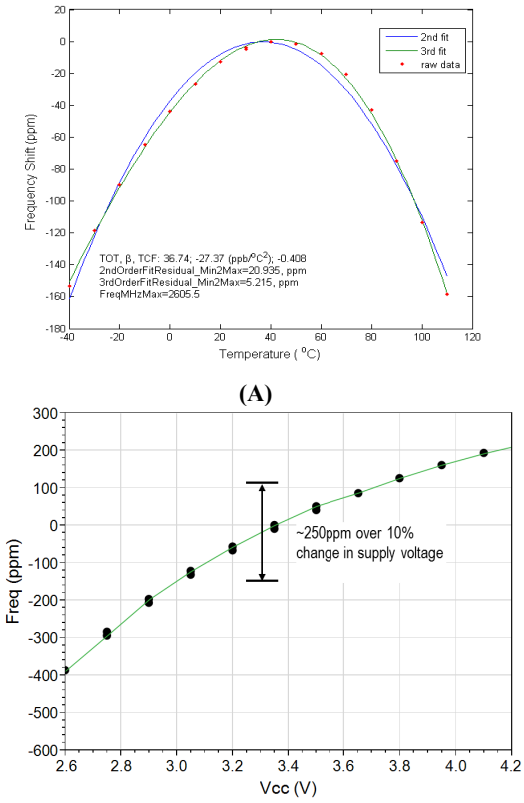


Figure 5: (A) Measured oscillator frequency drift as a function of temperature. (B) Measured oscillator frequency variation as a function of supply voltage.

Different applications of this technology will lead to different optimal partitioning. For example, a high-performance PLL could use the ZDR/bipolar chip as a low noise VCO with the digital functionality integrated onto a separate CMOS chip. We used bipolar devices for three reasons: first, this process has a higher f_T than comparable legacy inexpensive CMOS processes. Secondly, the lower 1/f noise of BJTs provides a significant improvement (6-8dB) in close-in phase noise. Finally, the gm/Id ratio is 2-3x higher than a MOSFET biased in strong inversion for high f_T.

Figure 6 shows the measured phase noise profile of the free-running oscillator when attached to three FBAR resonators of different frequencies, all with a high Rp stack (1.7, 2.6, and 3.4 GHz). We achieved better than -143 dBc/Hz phase noise at 1 MHz and an integrated jitter of 44 fs across all oscillators. As expected, the phase noise is degraded by approximately 6 dB when frequency doubles (from 1.7 GHz to 3.4 GHz).

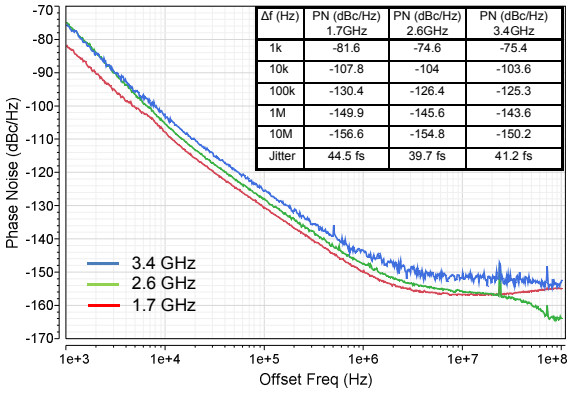


Figure 6: Phase noise of the oscillators with 3 resonators of 1.7, 2.6, and 3.4 GHz respectively, measured with an Agilent 5052 signal source analyzer.

The on-die varactor is used to pull the resonant frequency of the oscillator to compensate for temperature drift as well as any frequency variation due to processing uncertainty. An oscillator pulling range of 800 ppm is measured with the voltage on the integrated varactor varying from 0.5 to 1.8 V (Fig. 7). We measure less than 2000 ppm spread in the oscillator frequency across wafer.

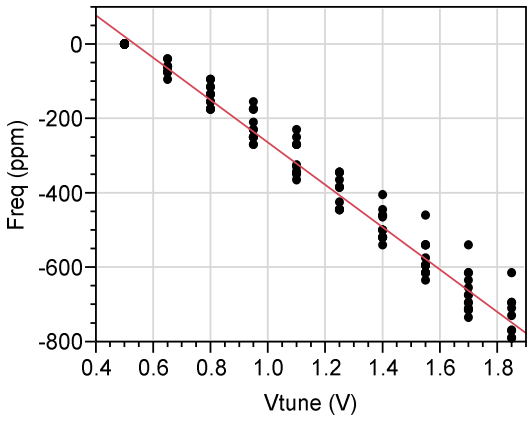


Figure 7: Measured tuning curve of ZDR oscillator.

Table 1 summarizes the performance of the 1.7 GHz oscillator implemented in this process and compares with related state-of-the-art. Since we are not targeting low-power applications, the current consumption of this work is higher than the prior work[5]. However, the far-off phase noise is better than reported previously.

V. Conclusions

We have presented a high-frequency, low-jitter frequency source using a ZDR-tuned oscillator implemented in a single-chip ZDR/bipolar process. A fully-differential oscillator allows large differential signal swings and achieves jitter as low as 25fs. The ZDR resonator is fabricated at the wafer level with the circuitry, which provides an extremely small form factor and (0.24 mm^3) minimal parasitics in a robust chip-scale package.

TABLE 1. DESIGN AND PERFORMANCE SUMMARY

	This Work	IFCS'10 [5]	ISSCC'06 [7]
Integrated FBAR	Yes	Yes	Yes
Hermetic	Yes	Yes	No
Freq (GHz)	1.7	1.5	5.4
Icc (μA)	1500	300	1700
Vcc (V)	3.3	1.8	2.7
L(1 kHz) dBc/Hz	-81.2	-80	-63
L(10 kHz) dBc/Hz	-107.8	-104	-93
L(100 kHz) dBc/Hz	-130.4	-124	-118
L(1 MHz) dBc/Hz	-149.9	-138	N/A

VII. References

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