A Low-Power Mixed-Signal Baseband System Design for Wireless Sensor Networks

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***Abstract*— We present the design methodology and a silicon implementation of a baseband system for use in wireless sensor network applications. Starting from the RF interface, our design process began with a system level phase inspired by the Platform-Based Design (PBD) methodology extended to the analog domain. The functional design was based on an Early-Late Gate synchronization scheme. The PBD approach was used to explore two alternative solutions: a predominantly digital one and a predominantly analog one. To validate the functional aspect of the design, a prototype implementation based on an FPGA and a Field Programmable Analog Array (FPAA) was derived using the PBD approach. Finally, we mapped the system level description to silicon aiming at an ultra low power implementation exploiting weak inversion in a 0.13μm CMOS process leading to an overall power consumption of 200μW with a 1V supply.**

I. Introduction

Recent progress in ultra-low power transceivers for sensor networks has reduced the receiver power consumption to below a milliwatt and the overall transceiver implementation volume to below 1mm^3 [1], [2]. This new radio utilizes a combination of micro-electromechanical (MEMS) devices and standard CMOS processes. The radio baseband (demodulation and synchronization) circuitry must be extremely small and exhibit very low power dissipation. This leads to fundamentally different baseband design approaches than the ones used in standard radios. To eliminate the need for replacing or recharging system batteries, all of the energy dissipated by the electronics must be scavenged from the environment [5],[6]. This limits the average power dissipation of the sensor node to around 100μW. One of the most challenging aspects of this vision is integrating a low power RF communication link capable of connecting the autonomous nodes into a large, ad-hoc network. This paper focuses on the demodulation synchronization hardware of such a system.

We believe that the constraints introduced above can only be met within a reasonable design time if a system level design methodology is used. In this paper, we report the results obtained using a design methodology based on an extension of Platform Based Design (PBD) to the analog domain, referred to as Analog-PBD (A-PBD) [3],[4]. A-PBD provides very efficient system level design exploration at high levels of abstraction where the analog and digital components can be easily interfaced. We define a *platform* as a library of components, each decorated with a set of methods to estimate performances and behavior and to provide correct ways of composing library elements. The design process advocated is *meet-in-the-middle*. First, a library of components (platform) is characterized bottom-up by extracting accurate models that include methods to compute physical quantities such as timing and power dissipation. This description of the components is used to offer the designer a way of exploring trade-offs when mapping the application to a legal composition of the platform components, called a *platform instance*. Because platform performances can be readily evaluated, efficient optimization can be carried out to perform design space exploration. The accurate performance models available with platforms guarantee implementability of selected performances so that design can proceed to the next level down the hierarchy.

In this paper we leverage the platform based approach to design the baseband section for the low power transceivers. We started with the Early-Late Gate synchronizer as a candidate algorithm and we built a platform consisting of analog and digital components for the implementation. In the first phase of the design we included in the library a Field Programmable Analog Array (FPAA) from Anadigm and a Xilinx FPGA so that rapid prototyping of the mixed signal design was possible. We performed two mappings on this platform, one with predominantly analog processing and another with mostly digital processing. After evaluating performances and extrapolating results to a custom design, we mapped the functional description of the design to an ultra-low power custom instance in 0.13μm CMOS consuming 200μW. The chip was successfully tested and is fully compliant with the system specifications.

II. System-Level Design

A custom RF transceiver operates at 2GHz and uses a simple ON/OFF keying (OOK) modulation scheme that proves to be very energy efficient for wireless sensor network systems [2]. An OOK modulation scheme allows simple detection on the receive side and efficient modulation on the transmit side. In addition, since the startup time of the transmitter is fast, the entire transmitter is cycled on/off between transmitted symbols. Thus, the entire transmitter is powered down while transmitting a zero, effectively reducing the energy consumption of the transmitter by a factor of two. The receiver, and thus the synchronizer, operates at 50kbit/s. An alternating 1010 training sequence header is used for synchronization. The goals of the synchronizer system are to maintain the inherent sensitivity of the receiver, demodulate the OOK data, minimize

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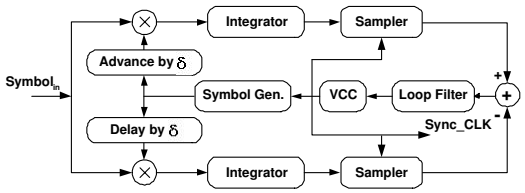

Fig. 1. Block diagram of Early-Late Gate synchronizer

the synchronization time, and operate at extremely low power consumption and bias current levels.

Fig. 1 shows the demodulator block diagram. The demodulator works by correlating the incoming signal with two copies of an internally generated symbol, one delayed by δ and one anticipated by δ. If the internal symbol clock is correctly synchronized, each integrator will integrate half of the symbol, so that no error signal is generated. If the symbol clock is leading (lagging), negative feedback is applied through combining the integration paths until synchronization is achieved [7]. This algorithm allows different implementations, ranging from a completely analog one (e.g. a principle implementation of the block diagram in Fig. 1) to a completely digital one (after the incoming signal has been sampled and converted). In this design, we explored the different possibilities of partitioning the design between analog and digital, evaluating performances as accurately as possible before final implementation on silicon. To achieve this, we modeled the algorithm at a high level of abstraction in Matlab/Simulink. We excluded the all-analog solution from exploration because we needed some flexibility in the control algorithm to adjust for variable bit rates. A mostly digital solution with digitization occurring immediately after down conversion, and a hybrid solution (predominantly analog processing) were investigated where signal processing is performed in the analog domain using a 1 bit converter (comparator) at the end of the sampler blocks to feed a digital control algorithm.

III. Prototyping

After validating the system at the functional level, it was mapped on the FPAA-FPGA prototype platform. Performance annotation was performed on the FPAA to introduce basic non-idealities so as to build an analog platform. However, the algorithm reported in Fig. 1 cannot be directly mapped on the FPAA because it is a switched capacitor fabric operated in the discrete time domain. In particular, restrictions on sample and hold instants imposed by FPAA clocks required adapting the synchronizer scheme as shown in Fig. 2. In the final implementation the input signal is low-pass filtered before informing two integrator paths, whose reset triggers are controlled by the FPGA. One path is delayed by one symbol period to implement an equivalent scheme to the δ delay in Fig. 1. Finally, a comparator determines the difference between paths. The digital control algorithm performs a binary search on the delay between the two paths by controlling the reset signal of the integrators. The refined system was then simulated and mapped on the platform. The analog

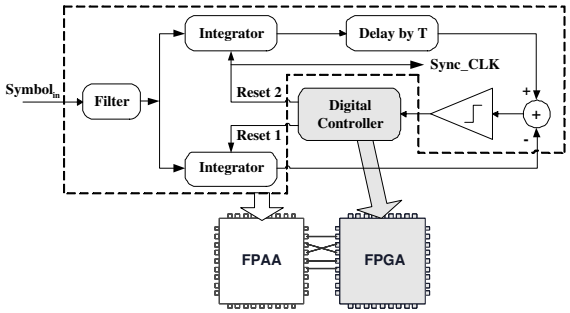

Fig. 2. Early-Late Gate synchronizer mapping on the FPAA-FPGA platform

block exploited the mapping tools provided by Anadigm that allow direct implementation of filters, amplifiers, and other functionalities. The digital controller, a finite state machine, was translated from Stateflow into VHDL with an in-house converter, and then the FPGA configuration was obtained through Xilinx tools. The platform selected for implementation is rich enough to allow implementing the alternate, mostly digital solution as well. We exploited the ADC available on the FPAA and a more complex finite state machine to perform synchronization, allowing a conversion speed of 1 MS/s with 8 bits of accuracy.

Both solutions were tested and interfaced with the custom low power receiver front-end. Overall, the hybrid solution performed better than the purely digital one, showing an improvement of sensitivity of 7dB over the digital implementation. In both cases, performances were limited by a DC offset that could not be removed without developing a custom board for testing. The hybrid solution was able to operate close to the sensitivity of the prototype receiver. Moreover, it allowed reconfigurability of the signal path in terms of filtering and gain so as to adapt to varying signal strengths and bit rates.

IV. Circuit Design

To meet the aggressive power consumption requirements of wireless sensor networks and to provide a solution suitable to the target node size, we performed another mapping of the Early-Late Gate synchronization algorithm starting from the hybrid solution, which showed encouraging results from the prototyping. We exploited the freedom of designing a custom circuit by choosing a continuous time implementation for the analog sub-system since this choice was likely to provide lower power consumption. Necessary adjustments were made to the functionality shown in Fig. 2. For example, we modified the third path to provide the carrier sense capability required by the MAC layer in the protocol stack by averaging 10 symbols. The final diagram is shown in Fig. 3.

The custom baseband chip was designed in a $0.13\mu m$ CMOS technology with 1.0V power supply. The analog circuits consist of integrators, a sample & hold, a track & hold, comparators and a precision-gain amplifier (Fig. 3). To minimize power consumption, weak inversion operating region was widely exploited throughout the circuit design. The platform based approach is able to efficiently exploit an

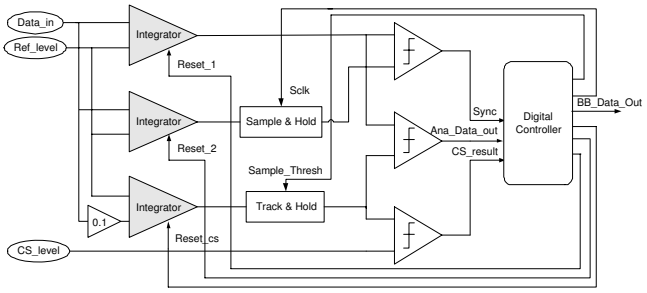

Fig. 3. Block diagram of the baseband silicon implementation

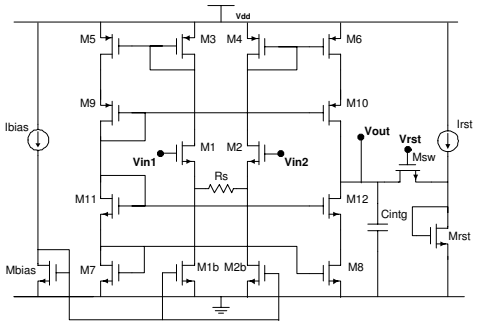

Fig. 4. Schematic of $G_m - C$ integrator

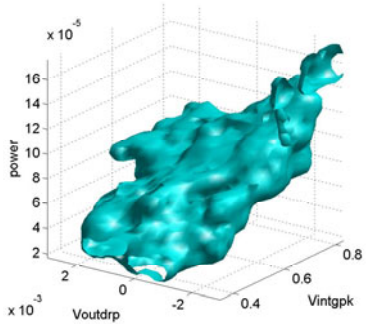

Fig. 5. Integrator performance space projection. The volume shows a feasible range of the integrator performance in terms of output voltage droop, integration peak level, and power consumption

enriched design space and provide an insight to the optimal regions of feasible performance, allowing designers to save time in sizing a given circuit to achieve an optimization goal. Consistent with analog PBD [3], a library of platform components was built to map the functionalities and perform design space exploration. One primary design challenge came from the integrators due to the relatively long integration time set by the system data rate (50kbps). In this section we will focus on the integrator design.

To maximize power efficiency, we adopted an $G_m - C$ structure integrator, where a CMOS OTA topology was designed as shown in Fig. 4. The synchronization scheme requires a maximum voltage droop of 2mV over one symbol period (20 μs). With the CMOS process used, a basic $G_m - C$ circuit fails because of excessive discharge rate of the integration capacitor due to the finite output impedance of the OTA. A cascode structure was utilized to increase the output impedance of the OTA and control the droop rate of the output node without resorting to unrealistically high values of integration capacitance. The integration gain is set by the integration capacitor (C_{intg}) and the OTA transconductance G_m, which can be easily tuned by changing the bias current and the sizing ratio between the loading transistors, M_3 and M_5, M_4 and M_6, as shown in the following equation.

$$\frac{dv_{out}}{dt} = \frac{i_{c_{intg}}}{C_{intg}} = \frac{G_m \cdot V_{in}}{C_{intg}} \quad (1)$$

To maximize the integration gain while maintaining the input dynamic range required by RF frontend, an optimization of the transconductance G_m was needed. As shown in (1), the integration gain can also be improved by choosing a relatively small C_{intg}. However, this will increase the output voltage droop. These tradeoffs needed to be carefully exploited. A-PBD techniques were used to optimize the circuit parameters and minimize power consumption. To characterize the circuit, we defined a feasible configuration space spanning from the integrator design parameters, considering the combination of different biasing, different device sizings and values of the integration capacitance (C_{intg}). Since the characterization cost is exponentially dependent on the size of these parameter combinations, to improve the characterization efficiency, a set of constraints was imposed to restrict the configurations, which include defining bounding ranges for devices size, defining biasing conditions, and using "long" low-leakage transistors for M_{9-12} to reduce the voltage droop. EKV models [8] were exploited to model the device operation and derive the constraints. Then, with the analog platform characterization framework [3], this configuration space was statistically sampled and circuit simulations were carried out in Spectre to obtain a feasible performance space as shown in Fig. 5. In this example, the performance space is in the dimensions of output voltage droop, integration peak level, which is proportional to integration gain, and power consumption. Using performance models, we carried out a preliminary exploration that allowed us to determine optimal regions in the feasible space. After that, to minimize the power consumption, local optimization of the circuit sizing and bias was carried out manually. This resulted in an optimized integrator current consumption of $16\mu A$ and $C_{intg} = 20pF$.

Another critical issue with the integrators is the reset path. All three integrators must be reset to the same constant level, independent of the integrated voltages. The potential solution of resetting the capacitor to a node of the OTA results in unacceptable time constants because of the large capacitor and the high impedance at that node. Instead, the integration capacitor is reset to a dedicated branch where a diode connected NMOS (M_{rst}) generates a reference voltage, at the expense of additional bias current.

Finally, to guarantee integrator gain matching and linearity matching between the first two integrator paths and the carrier-sense path, the same integrator cell was used on all paths, and a dedicated preamplifier was designed to attenuate the

input signal by a factor of 10. The comparator topology comprises a fully differential preamplifier followed by a CMOS latch [9] and a cross-coupled S-R latch. In this mixed-signal baseband, the digital controller consisted of a finite state machine synthesized using standard flows. Finally, we verified the implementation by conducting co-simulation of analog circuits and the digital controller.

V. Experimental Results

The die photograph is shown in Fig. 7. The chip area is pad limited to 2.0mm^2 (the active die area is 0.8mm^2). System-level tests were performed using the measurement setup shown in Fig. 6. A Rohde & Schwarz RF signal generator synthesizes the transmitter, which is driven by square wave modulation. The custom transceiver chip [1] is set in receive mode. The output of the receiver is fed into the mixed-signal baseband. A Xilinx FPGA is used to generate the 500kHz clock and system reset signal for the baseband and a 25kHz square wave modulation signal to drive the transmitter, which produces the RF signal of 2GHz. The data output from baseband is fed back to the FPGA and compared to the original modulation signal. This provides synchronization verification and bit error rate (BER) testing capability.

Fig. 7 shows the baseband operation with the radio after synchronization is successfully achieved. The first waveform shows the noisy input data stream (50kbps) with amplitude of around 20mV. The reset signal to the first integrator is shown as the second waveform. The synchronization is successful if this reset signal has the same timing as the rising (or falling) edge of input data. The last waveform is the data output from the baseband. As designed, there is a one-bit delay between the input and output data. The synchronization header length is 10 bits for amplitude estimation and 25 bits for timing estimation in the worst case. The minimum input level is around 20mV, which is limited by the integrator offset. Based on the measurement setup, the baseband is able to synchronize down to the sensitivity of the transceiver (-78dBm).

Using the internally-generated biasing, the analog circuits draw 180μA of current from the 1.0V supply, and the digital part draws 13μA. By externally setting lower bias currents, the baseband is still able to synchronize with a power consumption as low as 120μW. Decreasing the data rate further reduces power consumption. At a 20kbps data rate the baseband consumes only 80μW. In addition, another possibility to cut down power consumption is by turning off the second path and the first comparator after synchronization as they are not needed after synchronization is achieved. This would result in a reduction in power consumption of around 25%.

VI. Conclusions

In this paper, we presented the design methodology and an implementation of a low power mixed-signal baseband system for wireless sensor networks. This design is inspired by the analog platform-based design method. In this paradigm, design proceeded by successive refinements and mapping, from the initial algorithm selection to a preliminary mapping on a reconfigurable prototype platform and finally to a silicon implementation for ultra-low power consumption. Both the prototype and the chip are operational, the latter exhibiting 200μW power dissipation obtained by exploiting weak inversion design. Our measurements showed that the baseband is able to synchronize down to the sensitivity of the transceiver.

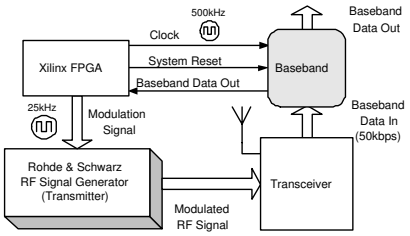

Fig. 6. Measurement setup

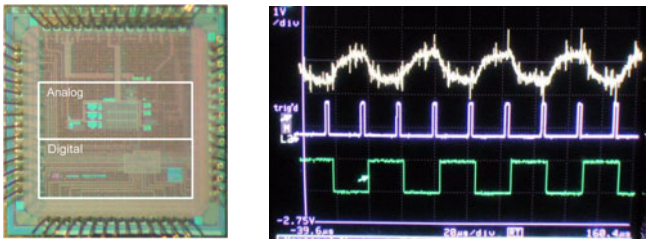

Fig. 7. Die photograph; Baseband operation with the radio after synchronization

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