A 300-μW 1.9-GHz CMOS Oscillator Utilizing Micromachined Resonators

Brian P. Otis, *Student Member, IEEE*, and Jan M. Rabaey, *Fellow, IEEE*

***Abstract*—A low-power low-phase-noise 1.9-GHz RF oscillator is presented. The oscillator employs a single thin-film bulk acoustic wave resonator and was implemented in a standard 0.18-μm CMOS process. This paper addresses design issues involved in codesigning micromachined resonators with CMOS circuitry to realize ultralow-power RF transceiver components.**

The oscillator achieves a phase-noise performance of −100 dBc/Hz at 10-kHz offset, −120 dBc/Hz at 100-kHz offset, and −140 dBc/Hz at 1-MHz offset. The startup time of the oscillator is less than 1 μs. The oscillator core consumes 300 μA from a 1-V supply.

***Index Terms*—MEMS, phase noise, RF oscillators.**

I. Introduction

As WIRELESS connectivity becomes progressively more widespread and portable in voice, data, and environmental monitoring applications, the power dissipation requirements for these systems become increasingly severe. In the field of sensor node networks, where the entire energy budget must be scavenged from the environment, the RF transceiver must dissipate less than a few milliwatts of power when active and demonstrate aggressive duty cycling and sleep modes [1].

To meet the stringent requirements of sensor node applications, the RF transceiver must utilize a sinusoid generator with extremely low power consumption, a fast startup time for agile duty cycling, and sufficient stability to maintain reliable connectivity.

A. Existing Solutions

Traditionally, the local oscillator (LO) signal is generated through frequency synthesis, which usually entails multiplying the frequency of a stable low-frequency crystal oscillator via a phase- or delay- locked loop (PLL or DLL) [2].

There are, however, several drawbacks with a frequency synthesizer. The low quality factor (Q) of the voltage-controlled oscillator (VCO) tank and finite loop bandwidth of the PLL severely degrade the inherent phase noise of the crystal oscillator. Additionally, the synthesizer consumes large amounts of power in the VCO and frequency dividers. In a recent ultralow-power frequency synthesizer design, approximately 400 μW was consumed to provide a 434-MHz carrier [3]. As the carrier frequency of these systems is increased into the gigahertz range, the power consumption of the frequency synthesizer increases dramatically. This problem is especially acute in sensor node radios, where a high carrier frequency is preferred to reduce the physical antenna size. The startup time of a traditional frequency synthesizer is relatively long, and can be inefficient if the transceiver requires aggressive duty cycling and short packet data transmission. Additionally, even with a fully integrated synthesizer, an off-chip quartz crystal is always required. Crystal oscillators typically exhibit very low phase noise due to the high quality factor of the crystal resonator. However, the resonant frequencies of quartz crystals are lower than most desired carrier frequencies, so frequency synthesis is usually required [4].

In this paper, an alternate method of sinusoid generation is used. A frequency reference is generated directly at the RF frequency of interest, with no low-frequency reference. This solution is not a VCO and operates without a PLL or crystal frequency reference, which implies that the oscillator is useful only for fixed frequency systems without stringent frequency stability requirements. This is accomplished by stabilizing a CMOS oscillator with an RF microelectromechanical (MEMS) resonator, ultimately combining the frequency stability of a mechanical resonance with the low power capability of standard submicron CMOS. Codesigning the resonator together with the CMOS electronics provides an extremely low-power solution.

B. FBAR Resonator

This oscillator uses a thin-film bulk acoustic wave resonator (FBAR) [5]. The FBAR employs a metal-piezo (AlN)-metal sandwich to achieve a high-frequency tightly controlled resonance with an unloaded series resonant Q of approximately 1200. As shown in Fig. 1, the resonator can be modeled as a series *LCR* circuit, with a series resonance occurring at $\omega_s = (L_x C_x)^{-1/2}$, where L_x and C_x are approximately 187 nH and 37 fF for this implementation, respectively. Capacitor C_o models a parasitic feedthrough capacitance created by the parallel plates of the resonator. In typical applications, FBARs are combined into ladder structures and used as duplexers and bandpass filters for wireless applications [6]. In this design, a single resonator is used to maximize the loaded Q of the oscillator. The resonator occupies approximately 100 μm$\times$ 100 μm and is wirebonded directly to the CMOS chip containing the circuitry.

II. Oscillator Design

A. Circuit Topology and Operation

A circuit schematic of the Pierce oscillator is shown in Fig. 1. The signal is dc coupled to the first stage of the output buffer (M_{buf1}). Capacitors C_1 and C_2 are necessary to achieve oscillation. In this implementation, no explicit capacitance was added and these capacitances are formed by the device, interconnect, and pad capacitances. Transistor M_{fb} acts as a large bias resistor. During oscillation, C_1, C_2, and C_o are tuned out, and M_1 sees a high impedance at its drain node. In the next section, the

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The authors are with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94704 USA (e-mail: botis@eecs.berkeley.edu; jan@eecs.berkeley.edu).

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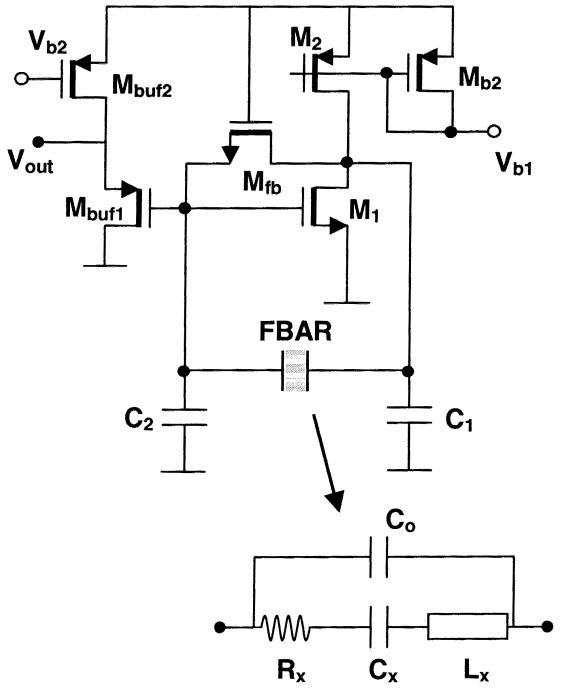

Fig. 1. Simplified oscillator schematic and FBAR resonator circuit equivalent model.

combined circuit/resonator is optimized to minimize the power consumption of the oscillator.

B. Resonator/Circuit Codesign

To achieve minimal power consumption, the CMOS circuitry and the resonant structure were jointly optimized. At resonance, the initial loop gain is

$$A_L = gm_1 R_L \frac{C1}{C2} \tag{1}$$

where R_L is the real impedance seen at the drain of M_1. It can be shown that optimal frequency stability and startup factor is achieved with $C_1 = C_2$ [7]. Therefore, to minimize the transconductance necessary for oscillation and to maximize the output voltage swing for a given bias current, R_L was maximized. For a given frequency, the FBAR resonator can be fabricated with various membrane areas. As the area increases, the motional resistance R_x decreases. However, increasing the area also increases the feedthrough capacitance C_o. Increasing R_x degrades the loaded Q of the oscillator, thus decreasing the R_L of (1). Increasing C_o has a similarly detrimental effect. Thus, it is possible to fabricate an optimal resonator area that minimizes the power dissipation and phase noise of the oscillator. Fig. 2 illustrates R_L versus resonator area, normalized to approximately 100×100 μm^2, for three values of $C_1 = C_2$. Using this technique, an optimal resonator area was chosen for fabrication. The curve marker in Fig. 2 indicates the design point. It is important to note that the finite Q of the CMOS device and pad capacitance must be considered, as they also reduce the loaded Q of the oscillator.

The desired voltage swing of the oscillator was 100-mV zero-to-peak. The following equation relates the desired voltage

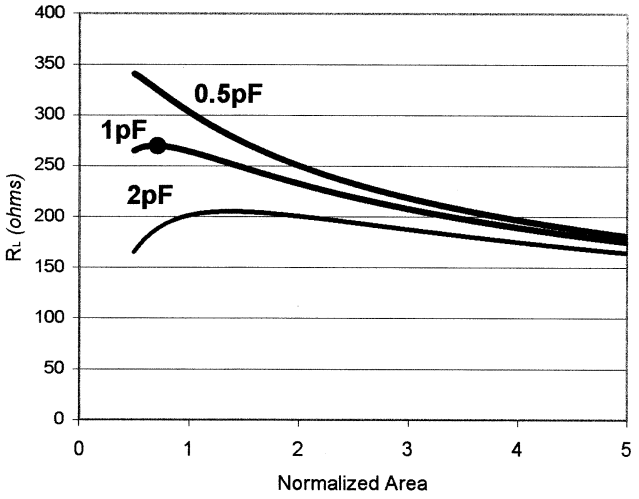

Fig. 2. Optimization of resonator area for three values of $C_1 = C_2$. The design point is indicated by the curve marker.

swing to the first harmonic component of the drain current of M_1:

$$V_o = I_1 R_L. \tag{2}$$

Given the ratio of $I_1/I_{\rm dc}$, which is determined by the operating region of M_1, the necessary oscillator core bias current was found to be approximately 300 μA.

Codesign and optimization of CMOS circuitry and RF MEMS components will become an increasingly important tool with the proliferation of this technology. The imminent integration of RF MEMS on the same silicon substrate as CMOS circuitry will enhance the performance of the system as well as the need for codesign.

C. Frequency Stability

This section explores the frequency sensitivity of the oscillator due to environmental effects and process variation of the CMOS and MEMS components. It can be shown that the oscillation frequency is

$$f_{\rm osc} = \frac{1}{2\pi\sqrt{L_X \frac{C_X C_T}{C_X + C_T}}} = f_{\rm series}\sqrt{1 + \frac{C_X}{C_T}} \tag{3}$$

where C_T is $(C_o + C_1 || C_2)$ and $f_{\rm series}$ is the series resonant frequency of the resonator. At the time of this writing, the fabrication tolerances on FBAR resonators are approximately $\pm$500 ppm [8]. Additionally, the temperature sensitivity of these resonators is around 25 ppm/°C [6]. Though sufficient for RF filter and duplexer applications, these tolerances are worse than crystal resonators, making an uncalibrated FBAR reference oscillator currently unsuitable for precision applications. These tolerances, however, are already sufficient as a frequency reference for certain low-power low-data-rate RF applications [1]. Given (3), the sensitivity of the oscillation frequency to capacitive variation can be derived as

$$\frac{\partial f_{\rm osc}}{\partial C_T} \cong f_{\rm series}\frac{-C_x}{2C_T^2}. \tag{4}$$

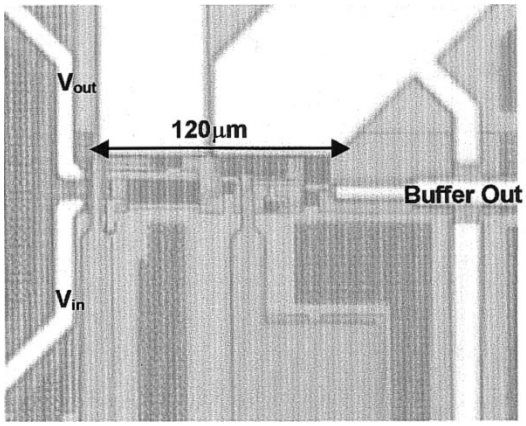

Fig. 3. Die photograph of CMOS oscillator core.

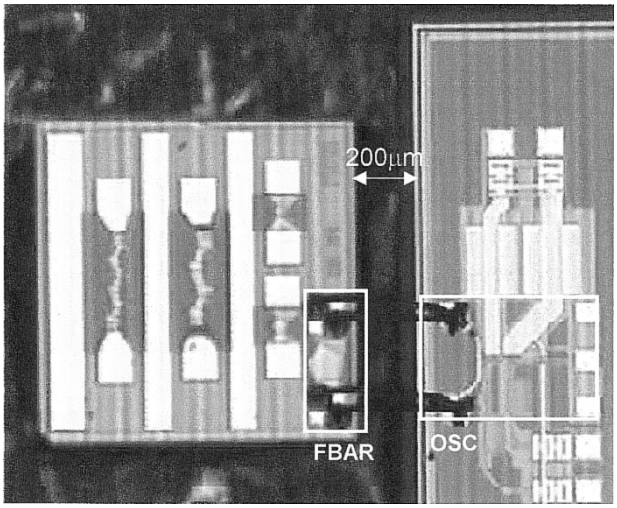

Fig. 4. Photograph of the CMOS oscillator wire bonded to the FBAR resonator.

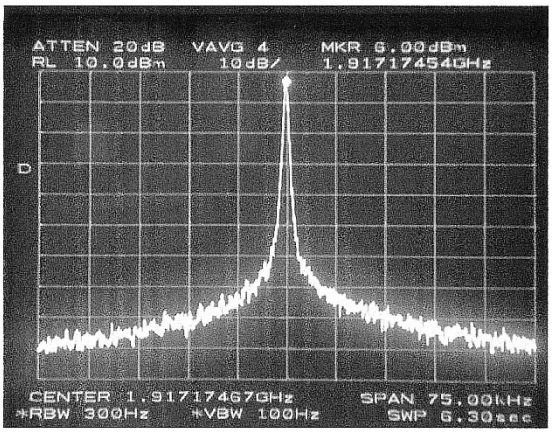

Fig. 5. Oscillator frequency spectrum.

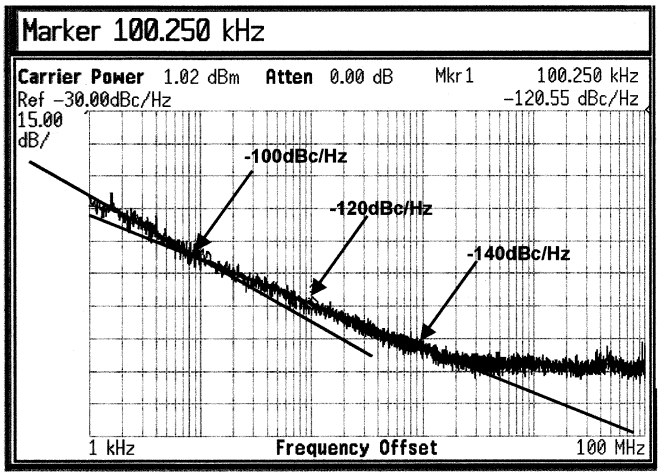

Fig. 6. Measured phase noise of the oscillator.

For this design, $\partial f_{\rm osc}/\partial C_T$ is approximately -10 MHz/pF, or over -5000 ppm/pF. It is, therefore, possible to tune the oscillation frequency with relatively small tunable or switchable capacitors, overcoming fabrication and temperature related process variations. This method has been utilized in precision crystal oscillator references [4]. It should be noted that increasing C_T to tune the oscillation frequency would load the resonator and result in increased power consumption.

III. Implementation

The oscillator was implemented in a standard 0.18-μm six-metal one-poly CMOS process, and is fully integrated except for one off-chip FBAR resonator. An on-chip two-stage buffer provides a low-capacitance dc-coupled interface to the oscillator and a 50-Ω interface to the output port (Fig. 3). Dual bondwires were used to minimize the inductance in the CMOS/MEMS interface (Fig. 4), and bondpads were constructed from M6–M5 layers with an M1 ground plane to minimize capacitance.

IV. Experimental Results

The oscillator core was biased at 300 μA with a power-supply voltage of 1 V. The frequency spectrum of the oscillator (Fig. 5) shows the oscillation at 1.9 GHz. Close-in spurs, indicative of parasitic low-frequency mechanical resonances, are absent in the output of the oscillator [9]. The amplitudes of the second, third, fourth, and fifth harmonics were measured to be 30, 36, 45, and 49 dB below the carrier, respectively.

The measured phase-noise performance is shown in Fig. 6. Phase noise was measured with an Agilent E4445A PSA and verified with an HP 3048A phase-noise measurement system. The measured phase noise of the oscillator is -100 dBc/Hz at 10-kHz offset, -120 dBc/Hz at 100-kHz offset, and -140 dBc/Hz at 1-MHz offset. This phase-noise performance is due to the high quality factor of the MEMS resonator. The startup time of the oscillator was measured to be approximately 800 ns, making it suitable as a frequency reference for receivers requiring agile duty cycling. For example, it is possible to cycle the oscillator on/off between transmitted bits for low-data-rate on/off-keying (OOK) modulation. In addition, it was experimentally verified that analog pulse shaping of the OOK envelope is possible by shaping the bias current of the oscillator as a function of time.

V. Conclusion

This paper presents a 1.9-GHz submilliwatt FBAR resonator-based CMOS RF oscillator. This oscillator is suitable for ul-

tralow-power RF transceiver applications such as sensor node networks. The oscillator dissipates 300 μW from a 1-V supply and achieves a phase-noise performance of -120 dBc/Hz at 100-kHz offset. To achieve better long-term frequency stability, it is possible to tune the oscillation frequency with variable capacitors. As shown in [10], it is also possible to implement a differential resonator-based oscillator to achieve better supply rejection and larger signal swings. The combination of standard CMOS and RF MEMS is shown to be a powerful tool in the design of ultralow-power RF transceivers.

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