A BAW-Enabled Low-Power 5X Frequency Multiplier

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Abstract—We present a low power Film Bulk Acoustic Wave Resonator (FBAR) enabled multiply-by-5 circuit. We compare its performance to a Q-enhanced LC tank-based multiplier for power, phase noise and carrier-to-spur ratio performance. The FBAR-based frequency multiplier (FM) provides 3 dB and 14.5 dB of phase noise filtering at 1 MHz and 10 MHz offsets, respectively, compared to an LC-based frequency multiplier. Due to its sharp roll-off, it improves spurious suppression by 14.5 dB. We implemented a prototype in 0.13 μm RF-CMOS process containing a multiply-by-5 and a differential ring oscillator. Each circuit consumes 700 μW while providing a 2 GHz output tone. The FBAR based FM provides a phase noise of −91.5 and −124.5 dBc/Hz at 1 MHz and 10 MHz offsets respectively while the phase noise for the LC tank based FM is −86.5 and −108.5 dBc/Hz.

I. INTRODUCTION

Miniaturization and power concerns, already important considerations in portable radio design, are amplified in emerging wireless sensor applications. High-Q resonators can significantly reduce the power dissipation of RF circuit blocks. Furthermore, utilizing high Q resonators can allow the realization of novel transceiver architectures. Passive impedance transformers, high-Q amplifiers, and deep notch filters providing high image rejection ratios can be realized [1]. With the help of a case study of BAW-enabled frequency multiplier, this article will explore the performance metrics that can greatly benefit from the use of high Q RF resonators: power, performance, and size. Here, we exploit the extremely high-Q filtering behavior of the FBAR device and present the design of a new frequency multiplier that allows the possibility of clean ultra low power clock sources for RF transceivers, data interfaces, and high speed ADC sampling clocks.

On-chip frequency multipliers (FM) find many applications in modern radio transceivers. For example, they allow the generation of very high frequency sinusoids beyond the $f_{\text{max}}$ of the technology [2]. The use of FM leads to wider spacing between the LO and RF frequencies, thereby reducing LO pulling, an important issue in zero/low IF receivers and direct conversion transmitters. Frequency multipliers become particularly attractive for mmWave applications [3]. In such applications, the quality factor (Q) of the tank is severely degraded due to poor varactor Q, resulting in phase noise degradation of fundamental frequency VCOs. Additionally, they suffer from narrower tuning range due to the fact that the parasitic capacitance leaves much less room for variable capacitance. Therefore, despite their inherent phase noise multiplication, frequency multiplication-based mmWave oscillators can compete with fundamental frequency oscillators in terms of phase noise while consuming less power and providing larger tuning range [5]. A power-efficient frequency multiplier can also be used to save power in synthesizers. This can be achieved by operating the LO and prescaler at $f_{\text{out}}/M$, where $f_{\text{out}}$ is the desired RF frequency and $M$ is the factor of multiplication.

In phase-locked loops, close to carrier VCO phase noise is filtered by the narrow-band loop transfer function. However, outside the loop bandwidth, the phase noise of the PLL output is primarily determined by the VCO phase noise. Reducing the VCO phase noise typically incurring a power penalty. In this paper, we present a low-power frequency multiplier circuit that employs a Film Bulk Acoustic Resonator (FBAR) to provide phase noise improvement without adding power. We compare its performance to a replica circuit using an LC tank as the FM filter. The rest of the paper is organized as follows. Section II summarizes existing literature on frequency multipliers. It also describes the principle of FM based on edge-combining. Section III contains a development of the low-power edge-combiner circuit used in our FM. Section IV presents measurement results, and conclusions are presented in Section V.

II. FREQUENCY MULTIPLICATION

Fig. 1. Block diagram of the FBAR based frequency multiplier using edge-combining.

Frequency multipliers based on harmonics of the fundamental tone are typically feasible only for low factors of multiplication as the power in the $n^{th}$ harmonic drops as $1/n^2$ [4] [5]. As a result, most existing FM circuits are practical only for small factors of multiplication such as 2 or 3. Similarly, the lock bandwidth of subharmonic injection locking used for frequency multiplication falls drastically with the factor of multiplication [5].
As shown in Fig. 1, edge-combining offers a robust method of frequency multiplication wherein low frequency equally spaced edges are combined to produce a high frequency sinusoid. This method does not place any fundamental constraints on the multiplication factor. However, practical considerations such as process variations will eventually impose a limit. These edges can be derived from a low frequency ring oscillator [2] or a delay-locked loop (DLL) [6][7].

Ring oscillators conveniently generate multiple phases, but suffer from degraded phase noise compared to LC-VCOs. To improve this, we have illustrated this technique for N=3, it can be easily extended to any odd number greater than 3 (5 in this work). Even though we have illustrated this technique for N=3, it can be used in a phase-locked loop (PLL) and subsequently fed to the FM edge-combiner. With this application in mind, it is imperative to develop a low-power edge-combiner. Inverter based ring oscillators have primarily dynamic power-dissipation and provide rail-to-rail swing, which can be taken advantage of to simplify the design of a low-power edge-combiner. Prior work [2][6] has used a differential amplifier-based ring oscillator/delay cell. Differential amplifiers do not provide rail-to-rail swings, requiring the edge-combiner to employ a differential MOS transistor pair as a unit for commutating the tail current. The tail current sources in these differential pair lead to increased static power consumption. The authors in [9] present a power efficient technique for edge-combining but exhibits a relatively low amplitude at the frequency multiplied output.

### A. FM using edge-combining

Consider a 3-stage ring oscillator and voltage waveforms at nodes A, B and C as shown in Fig. 2(a). Signals AB, BC and CA, represent the logical ANDing of the waveforms, and are displaced from each other by T/3, where T is the time period of the ring oscillator. If we combine the equally spaced signals (by wire-ORing them), the resultant waveform will be periodic with period T/3. An efficient method to perform this logical ANDing is to use MOS transistor switches in cascade as shown in Fig. 2(b) [7]. The current from each pair of switches then flows through the LC tank tuned at 3fRO, where fRO is frequency of the ring oscillator. The tank filters out the frequency components other than the fundamental (Fig. 2(b)). Even though we have illustrated this technique for N=3, it can be easily extended to any odd number greater than 3 (5 in this work).

### III. FBAR based edge-combiner circuit

The LC-tank used to filter current harmonics can be replaced with an FBAR resonator (Fig. 2(b)). This helps eliminate the huge area of the on-chip inductor (=300μm x 300μm) while providing extremely high Q (=2000). Fig. 3(a) shows the 6-element modified Butterworth-Van Dyke (mBVD) model [10] for a 2 GHz FBAR. Fig. 3(b) shows simulated impedance profiles of the loaded FBAR and LC tanks tuned at 2 GHz. The loaded FBAR exhibits a comparable parallel resistance Rf and a highly steep roll-off. At 1 and 10 MHz offsets, the loaded FBAR provides 6.5 and 25 dB attenuation, respectively, leading to filtering of close-in phase noise without extra power.

We have implemented a differential version of the edge-combiner circuit that employs edges from a differential ring oscillator based on inverters [8]. Fig. 4(a) shows the five stage (each stage consisting of 3-inverters) voltage controlled PMOS transistor as shown in Fig. 4(b).

Fig. 5(a) and 5(b) depict edge-combining FM circuits using an on-chip LC tank and FBAR resonator respectively. Switch matrices S and S̄ (shown in Fig.6(a) and 6(b) respectively) derive their edges from the differential ring oscillator. Since the FBAR presents a capacitive load at DC, the cross-coupled top PMOS transistor pair leads to latch up. The resistive biasing arrangement fixes the common-mode point. The cross-coupled PMOS pair in the LC-FM provides negative gm and thus enhances the tank Q. To compare their performance, both circuits were fabricated in 0.13 μm RF-CMOS process for a multiplication factor M=5 and a 2 GHz center frequency.
Assuming that the edge-combiner injects square current pulses into the resonant load, the differential signal amplitude at the frequency multiplied output is given by

\[ V_{amp} = \frac{4}{\pi} I_{tail} R_P \]  

Where \( I_{tail} \) is the tail current and \( R_P \) is the load impedance at resonance. Using \( R_P = 1.5 \, k\Omega \) and \( I_{tail} = 200 \, \mu\text{A} \), \( V_{amp} \) becomes 382 mV. Without any filtering being applied at the output, the phase noise at frequency multiplied output will degrade by \( 20\log_{10}M \) (14 dB). For the FBAR-FM, we expect phase-noise filtering due to the high resonator Q, resulting in less than 14 dB degradation above 1 MHz (3 dB bandwidth of the FBAR).

### IV. MEASUREMENT RESULTS

The differential ring oscillator is tunable from 396 MHz to 460 MHz (1.98 GHz-2.30 GHz at the FM output) with a 1.2V supply (Fig. 7(a)). Fig. 7(b) shows the phase noise of ring oscillator at 1 MHz and 10 MHz offsets.

Fig. 8 and 9 show the measured phase noise profiles of the open loop ring oscillator and frequency multiplied outputs, respectively. For \( M=5 \), the frequency multiplier phase noise degradation is theoretically 14 dB which is observable in the LC based FM as the low Q of LC tank does not offer any significant phase noise filtering. Similarly, at low offsets, the phase noise of FBAR-FM is also degraded by 14 dB. However, due to the very high quality factor of the FBAR resonator (\( Q > 2000 \)), the steep roll-off results in a phase noise improvement by nearly 3 dB and 14.5 dB at 1 MHz and 10 MHz offsets, respectively.

Fig. 10 shows the measured normalized frequency response of the loaded LC and FBAR resonators used in the FM circuits. Fig. 11 captures the measured time domain waveforms of the ring oscillator and FM output showing multiplication by five.

Mismatches between inverters in the ring oscillator lead to delay mismatches between adjacent phases. This, in turn, leads to spurs in the frequency multiplied output at frequencies \( M \pm \)
Fig. 11. Measured time-domain waveforms of the ring oscillator and frequency multiplied output for FBAR-FM circuit.

Fig. 12. Carrier-to-spur ratio for the LC based FM.

Fig. 13. Carrier-to-spur ratio for the FBAR based FM.

Fig. 14. Micrograph of the chip implemented in 0.13 μm technology.

\[ n f_{RO}, n = \pm 1, \pm 2 \ldots \] The tones at \((M \pm 1) f_{RO}\) are the most critical as they experience much less attenuation from the band-select filter. Fig. 12 and Fig. 13 show a carrier-to-spur ratio (CSR) for the LC and FBAR based FM circuits respectively.

Fig. 14 shows the prototype chip implemented in 0.13 μm RF-CMOS process. The active area used by LC-FM is 350 μm × 450 μm and is dominated by a 300 μm × 300 μm inductor. The active area used by FBAR-FM is only 70 μm × 25 μm. Table I summarizes the performances of LC and FBAR based FMs for the same power dissipation and output amplitude. Each ring oscillator draws about 450 μA of current from 1.2 V supply while the FM draws 200 μA from 0.8 V.

V. CONCLUSION

We have introduced a new FBAR-based frequency multiplier. This circuit outperforms a comparable LC tank based multiplier in terms of close-in phase noise and carrier-to-spur ratio. Measurement results for a multiply-by-5 circuit at a 2 GHz output frequency show that the FBAR-based FM circuit achieves a 3 dB and 14.5 dB phase noise improvement at 1 MHz and 10 MHz offsets respectively. Compared to the LC-FM, the FBAR-FM also provides 14 dB improved CSR. Each circuit consumes about 700 μW of power while providing a 2 GHz output tone.

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REFERENCES


TABLE I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>FBAR-FM</th>
<th>LC-FM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total power consumption</td>
<td>700 μW</td>
<td>700 μW</td>
</tr>
<tr>
<td>Phase noise of ring oscillator (dBc/Hz) at 10 MHz offset</td>
<td>-124</td>
<td>-123.8</td>
</tr>
<tr>
<td>Phase noise at FM output (dBc/Hz) at 10 MHz offset</td>
<td>-124.5</td>
<td>-108.5</td>
</tr>
<tr>
<td>Phase noise improvement at 1 MHz offset (dB)</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>Phase noise improvement at 10 MHz offset (dB)</td>
<td>14.5</td>
<td>0</td>
</tr>
<tr>
<td>CSR (dB)</td>
<td>37.7</td>
<td>23.7</td>
</tr>
</tbody>
</table>