A 220dB FOM, 1.9GHz oscillator using a phase noise reduction technique for high-Q oscillators

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Abstract—We present a technique to reduce the close-in phase noise of high-Q (FBAR/MEMS/crystal) oscillators. The proposed technique suppresses the up-conversion of 1/f noise via AM-PM conversion by the addition of a non-linear capacitor to the tank. The proposed AM-PM suppression technique has no additional power penalty and incurs a minimal area penalty. Measurements from multiple dies of a 1.9GHZ FBAR oscillator show ≥3.5dB reduction in close-in phase noise using the proposed technique. The FBAR oscillator achieves a measured phase noise of -88dBc/Hz @ 1kHz, -116dBc/Hz @10kHz, -146dBc/Hz @ 1MHz offsets. The oscillator with the proposed technique achieves a Figure of Merit (FOM) of 220dB, which is 5.5dB better than the FBAR oscillator with lowest close-in phase noise reported to date [1].

I. INTRODUCTION

Wafer scale high-Q MEMS resonators are becoming attractive alternatives to quartz owing to their small size, low cost and integration potential[2]. Thermal stability of MEMS based references has also improved to sub-ppm levels in the recent past[3].

Measurements from a fabricated 1.9 GHz FBAR oscillator show a 4 dB reduction in close-in phase noise with no power penalty, using the proposed AM-PM suppression technique.

The proposed AM-PM suppression technique is demonstrated using an FBAR oscillator but applicable to any oscillator employing a high - Q resonator.

The paper is organized as follows. Section II describes the proposed AM-PM suppression technique. Section III describes the circuit implementation and Section IV gives the experimental results and compares our oscillator with previously published FBAR oscillators.

II. PROPOSED AM-PM SUPPRESSION TECHNIQUE

We use the Pierce oscillator topology shown in Fig. 2 as a test vehicle for the proposed technique. One can model the oscillator as shown in Figure 2b, where the active circuitry is replaced by a capacitor and negative resistance connected across the FBAR. $C_{eff}$ and $R_{eff}$ are large signal parameters and are nonlinear in a typical oscillator.

A. AM-PM conversion

Large voltage swings at node X and Y in Fig.2, which are desirable for low far-out phase noise, cause transistors MP and MN to span multiple operating regions. This makes the gate and drain parasitic capacitances non-linear, thereby making $C_{eff}$ nonlinear. Any $\frac{1}{f}$ noise in the bias current of the oscillator modulates the oscillation amplitude (AM) and
hence modulates $C_{eff}$. This leads to frequency modulation of the oscillator, generating phase noise. This up-conversion of $\frac{1}{2}$ noise into phase noise through capacitance non-linearity, is the well known AM-PM phase noise generation mechanism in oscillators. We can estimate the phase noise due to AM-PM conversion using the following formula [8].

$$L_{AM-PM}(\omega_m) = \frac{1}{2} \frac{\partial \omega}{\partial I_{bias}} \frac{S_1(\omega_m)}{\omega_{m}^2}$$  \hspace{1cm} (1)

Where $S_1$ is the PSD of the noise in the bias current, $\omega_m$ is the offset at which phase noise is measured, $\omega$ is the oscillation frequency and $I_{bias}$ is the oscillator bias current. We estimate the term $\frac{\partial \omega}{\partial I_{bias}}$ from large signal periodic steady state (PSS) simulations of the Pierce oscillator and plug it in eq.(1). Figure.3 compares the total simulated phase noise of the oscillator with the phase noise estimated from eq.(1). We see that AM-PM conversion accounts for almost all of the phase noise at low frequency offsets, and hence is the dominant close-in phase noise generation mechanism for an FBAR oscillator. This mechanism is similar to the varactor non-linearity discussed in [10] except the non-linearity arises from device parasitics and not from explicitly added varactors.

In contrast to an FBAR oscillator, the dominant close-in phase noise mechanism in LC oscillators is the incremental Groszkowzki’s effect [8]. Phase noise due to incremental Groszkowski’s effect is derived in [8] as

$$L_{Groszkowski}(\omega_m) \propto \frac{1}{Q^4}$$

FBAR/MEMS/Quartz resonators have more than two orders of magnitude higher Q compared to on-chip LC tanks. Hence, phase noise due to Groszkowski’s effect is heavily suppressed in high-Q oscillators.

To suppress this AM-PM up-conversion, the designer should strive to reduce $\frac{\partial \omega}{\partial I_{bias}}$, i.e. make the oscillation frequency independent of bias current around the operating point of the oscillator. We can write

$$\frac{\partial \omega}{\partial I_{bias}} = \frac{\partial \omega}{\partial C_{eff}} \frac{\partial C_{eff}}{\partial I_{bias}}$$  \hspace{1cm} (2)

The term $\frac{\partial \omega}{\partial C_{eff}}$ is constrained primarily by the resonator and is typically not a degree of freedom for the circuit designer. But the term $\frac{\partial C_{eff}}{\partial I_{bias}}$ can be manipulated to reduce $\frac{\partial \omega}{\partial I_{bias}}$. For the oscillator in Fig.2 we can write

$$C_{eff} = C_{fixed} + C_{par}$$  \hspace{1cm} (3)

$C_{fixed}$ is made of the explicitly added capacitors $C_d$ and $C_g$. $C_{par}$ is made up of parasitics of MP and MN. One can use linear MIM capacitors for $C_d$ and $C_g$, thereby making $C_{fixed}$ linear. $C_{par}$ is typically non-linear and varies with bias conditions and voltage swing. From eq.(3) we can write.

$$\frac{\partial C_{eff}}{\partial I_{bias}} = \frac{\partial C_{fixed}}{\partial I_{bias}} + \frac{\partial C_{par}}{\partial I_{bias}} \approx \frac{\partial C_{par}}{\partial I_{bias}}$$  \hspace{1cm} (4)

Typically, $C_{par}$ is defined by the width and length of MP and MN, which are chosen with other considerations in mind (power consumption,far-off phase noise, oscillator swing etc). So the designer does not have any degree of freedom to reduce $\frac{\partial C_{par}}{\partial I_{bias}}$. To provide the required additional degree of freedom to the designer, we add a compensation capacitor $C_{comp}$. The new effective capacitance is

$$C_{eff}' = C_{fixed} + C_{par} + C_{comp}$$  \hspace{1cm} (5)

If we chose

$$\frac{\partial C_{par}}{\partial I_{bias}} = -\frac{\partial C_{comp}}{\partial I_{bias}}$$  \hspace{1cm} (6)

we can write

$$\frac{\partial C_{eff}'}{\partial I_{bias}} = \frac{\partial C_{par}}{\partial I_{bias}} + \frac{\partial C_{comp}}{\partial I_{bias}} \approx 0 \implies \frac{\partial \omega}{\partial I_{bias}} \approx 0$$  \hspace{1cm} (7)

By choosing an appropriate non-linear compensation capacitor $C_{comp}$ the designer can desensitize the oscillation frequency with respect to the bias current, thereby suppressing AM-PM conversion. In our design $C_{eff}'$ increases with the bias current and voltage swing. This increase in capacitance is primarily caused by the increase in drain-bulk diode capacitance of MN. So we choose a $C_{comp}$ made up of zero-VT NMOS transistors shown in Figure.4. $C_{comp}$ decreases with increasing oscillation amplitude, cancelling the increase in $C_{par}$. We size the NMOS transistors in Fig.4 to satisfy eq.(6).
mean value of the capacitances are subtracted out to bring out the compensation more clearly. We see that the slope of $C_{eff}^\prime$ is much smaller than that of $C_{eff}$. With a reduced $\frac{\partial C_{eff}^\prime}{\partial I_{bias}}$, we see a suppression in the simulated close-in phase noise. Fig.6 shows the achieved close-in phase noise suppression in simulation.

It may appear that a simple reduction in flicker noise in the bias path will reduce close-in phase noise, obviating the proposed scheme. This is not the case, and it should be noted that the proposed scheme is complementary to flicker noise reduction in the bias circuit. Referring to eq.(1), the proposed scheme reduce $\frac{\partial \omega}{\partial I_{bias}}$, while one can independently reduce the bias noise $S_I$. In fact, for a given target phase noise, the proposed technique simplifies the bias circuit design, by relaxing its noise specification.

To experimentally verify our AM-PM suppression technique, we fabricated the test circuit shown in Fig.7. MP1 and MN1 form a Pierce oscillator. The compensation capacitor is made of two zero VT NMOS sized $\frac{2 \mu m}{2 \mu m}$. The mean value of $C_{comp}$ is 60 fF. A digital control $D_{comp}$ selects either $C_{comp}$ or $C_{MIM}$, a linear 60fF MIM capacitor to be connected across the FBAR. This enables us to turn the compensation ON and OFF, without affecting the total tank capacitance and other oscillator parameters.

A digitally programmable bias circuit controlled by $D_{BIAS}$ biases MN1, providing an experimental knob to vary the current through the oscillator. The oscillator is followed by a multi-stage buffer made of transistors MN2-MN6, MP2-MP3 and multiple CMOS inverters to square up the signal. The last stage is an open drain buffer feeding the output pads. The oscillator core occupies an area of $250 \mu m \times 100 \mu m$. The oscillator nominally operates at a $V_{dd}$ of 1.2V and consumes a bias current of 1.3mA.

IV. EXPERIMENTAL RESULTS

The oscillator circuit was fabricated in 0.13 $\mu$m IBM CMOS 8RF process. The CMOS oscillator is wire bonded to an 1.9GHz FBAR from Avago Technologies. Fig. 8 shows the board assembly of the CMOS oscillator and FBAR.

To experimentally verify whether the proposed compensation reduces the term $\frac{\partial \omega}{\partial I_{bias}}$, we measure the oscillation frequency across bias currents, with and without the compensation. Fig.9 shows that the oscillation frequency becomes 2.7X less sensitive to the bias current, when the compensation is turned on.

Fig. 10 shows the measured phase noise with and without the AM-PM suppression. Turning the compensation on reduces the close-in phase noise by 4 dB while retaining the far-off phase noise at the same value. We measured the phase noise performance of the oscillator on 4 different dies. We consistently observed a $\geq 3.5$dB reduction in phase noise in all 4 dies using the proposed technique.

While a 2.7X reduction in $\frac{\partial \omega}{\partial I_{bias}}$ must correspond to 8dB reduction in phase noise, we measure only a 4 dB reduction. This indicates that the presence of phase noise from another mechanism at 7dB lower than the dominant AM-PM mechanism. This mechanism becomes the next dominant source of phase noise once the AM-PM up-conversion is suppressed by
8 dB. Further experimental work is required to identify and address this mechanism.

Figure 11 shows the screen shot of the measured phase noise of the oscillator at a Vdd of 1.2 V and bias current of 1.3mA. With the compensation turned on, we achieve a phase noise of -88 dBc/Hz at 1kHz, -116.3 dBc/Hz at 10 kHz and a noise floor of -146 dBc/Hz.

Fig. 11. Measured phase noise of the oscillator

In Table I we compare the proposed oscillator with other previously published FBAR oscillators[11][12][13][1][7]. The Figure Of Merit (FOM) is computed at 10kHz offset as this study focused on close-in-phase noise. We see that the proposed technique enables the oscillator to achieve an FOM of 220dB, which is 5.5 dB better than the FBAR oscillator with the lowest close-in phase noise reported to date [1]. The oscillator in [11] achieves a 2 dB better FOM than this oscillator. However [11] achieves this FOM by drastically trading off phase noise for an ultra low power consumption, while this work achieves a comparable FOM by improving the phase noise using the AM-PM suppression technique.

V. Conclusion

This work experimentally confirms that the dominant source of close-in phase noise in high-Q FBAR oscillators is the AM-PM up-conversion arising from non-linear device parasitics. A non-linear compensation capacitor added across the tank improves phase noise by ≥ 3.5 dB. The proposed compensation technique enables the 1.9 GHz FBAR oscillator to achieve a phase noise of -88dBc/Hz at 1kHz and an FOM of 220 dB.

REFERENCES


