# Microscale Silicon Thermoelectric Generator with Low Impedance for Energy Harvesting

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## Abstract

Research conducted on silicon micro thermoelectric generators (µTEGs) has shown promise for monolithic integration of environmental energy harvesters with power electronics, sensors, and radio transceivers. Unfortunately, the series electrical resistance of silicon microgenerators fabricated to date is too large to drive ultra-low power electronics. We have demonstrated the feasibility of a suspended-membrane silicon µTEG fabricated on a silicon-on-insulator (SOI) substrate in a bulk process. Unlike previous work, our in-plane thermoelements can be lithographically defined. Device simulations predict an output of 11 µW at 400 mV to a matched load, given a 10 K thermal gradient across a 1x1 mm$^2$ device with generator resistance of 15 kΩ. This technique provides the potential for thermoelectric generators that can be monolithically integrated with electronics.

## Introduction

Energy harvesting systems with power source, sensors, and communications on a single die will give rise to low-cost, batteryless solutions to a range of current problems in the medical, instrumentation, and commercial industries. Heat is an abundant environmental energy source and is converted to electricity via the Seebeck effect. The Seebeck coefficient of a material is generally measured in µVK$^{-1}$. By connecting a number of thermocouples electrically in series and thermally in parallel, thermoelectric generators can drive electric loads though the energy conversion efficiency is typically low as given by the Carnot efficiency in the equation below,

$$\eta_c = (T_h - T_c) / T_h . \qquad (1)$$

Promising application areas for microscale thermoelectric generators include on-board power sources for underwater, soil, automotive, and biological sensors. Silicon-micromachined generators have been a part of the micro thermoelectric device literature, but compound semiconductor materials (notably Bi$_2$Te$_3$ in room temperature applications) that have been shown to have relatively high conversion efficiencies have seen more development [1-4]. Poly-silicon generators with more than 10$^4$ elements per device have recently been fabricated in an augmented BiCMOS process [5,6]. The relatively large number of thermocouples is necessary to reach voltage sufficient to drive conventional electronics due to the small thermal gradient available to the thermocouples with effective lengths limited by a thin-film oxide layer. The electrical resistance for the generators is on the order of MΩ, almost half of which is due to the metal-semiconductor contact resistance the thermocouples.

## Materials Consideration

Generators fabricated with Bi$_2$Te$_3$ and related compound semiconductors have a figure of merit (FOM) more than an order of magnitude greater than silicon. The thermoelectric FOM is defined as

$$Z = \alpha^2 / \lambda\rho \ \ [K^{-1}], \qquad (2)$$

where $\alpha$ is the material-dependent Seebeck coefficient (µVK$^{-1}$), $\lambda$ is the thermal conductivity (Wm$^{-1}$K$^{-1}$), and $\rho$ is the electrical resistivity (Ω cm). While these more exotic semiconductors generally have much lower thermal conductivities than silicon, they have not to date been integrated with CMOS processes making cofabrication of the generator with circuitry implausible.

Silicon has a large magnitude Seebeck coefficient in the range of 100-1000 µVK$^{-1}$ depending on dopant levels [7,8]. At optimum doping levels (~10$^{19}$cm$^{-3}$) this represents more than double the Seebeck voltage of Bi$_2$Te$_3$ given the same thermal gradient. This property is an important consideration. Despite silicon's high thermal conductivity which keeps its FOM low, many candidate circuits require only a few hundred mV to operate, making silicon a viable choice as the generator material. Further, the problem of large numbers of thermoelements and associated excessive generator resistance of other silicon generator designs can be alleviated by using lithographically defined, planar thermoelements. The resulting lateral heat flow must be isolated, defining a heat source and sink bridged by the thermoelements, in order to get an appreciable thermal gradient across the generator. Simulations of on-membrane structures have established a theoretical basis for microgenerators of this topology [9].
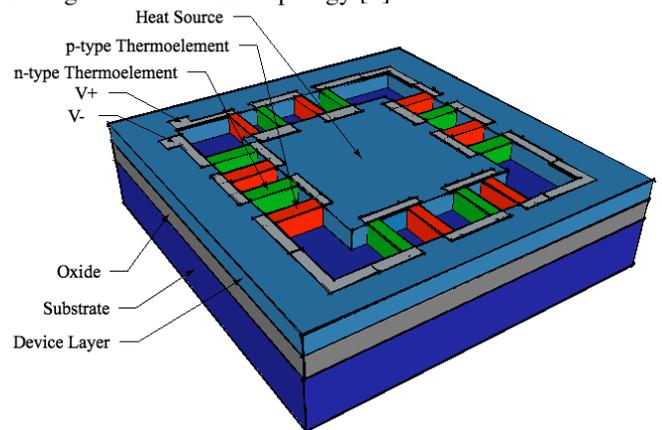


Figure 1: SOI-µTEG device conception. Heat flows from suspended membrane through parallel thermoelements to rim, oxide, and substrate.

## Device Conception

Our thermoelectric generator is to be fabricated on a standard silicon-on-insulator (SOI) substrate. The parts of the device are the substrate, the oxide, and the active or device layer, from which the device's rim, thermoelements,

and suspended membrane are fabricated (Fig. 1). The membrane acts as the heat source and the substrate as the heat sink with heat flow through the thermoelements, the rim, and the oxide layer. While the oxide acts to decrease the thermal gradient available across the thermoelements, its thermal resistance is small due to its large cross-sectional area. Once etched away it provides thermal isolation between the membrane and the substrate.

## Simulations

We have simulated the thermal and electrical performance of a range of SOI-µTEG devices. We used Comsol Multiphysics and Matlab for the simulations and have varied several parameters: overall module length, membrane width – which determines the resulting thermoelement length, and thermoelement width. The module lengths for the simulation are 500 µm, 1 mm, and 2 mm. The width of the rim is set as one twentieth of the overall module width. The membrane area is toggled between 60% the width of the module and 80% the width of the module. While increasing the area of the membrane decreases the length of the thermoelements, it increases the number of thermocouples that can bridge the rim to the membrane. The leg widths in the simulation are varied from 200 µm to 5 µm with a minimum interleg spacing of 5 µm. The number of thermocouples for each device is

$$n = 4\,\text{floor}[L_{mem} / 2(W_{leg} + W_{il})] \qquad (3)$$

where $L_{mem}$ is the length of the membrane, $W_{leg}$ is the width of the thermoelectric legs, and $W_{il}$ is the interleg width between thermoelements.

The thicknesses of the substrate, oxide and device layers are considered fixed for this work at 500 µm, 1 µm, 5 µm, respectively. Material properties for these layers were chosen from commercially available wafers, with special consideration given to a high resistivity device layer of 4 kΩ cm to avoid parasitic resistive coupling between adjacent thermocouples. Electrical resistivity, thermal conductivity, and Seebeck coefficient values for the thermoelements were taken from the literature to correspond to a doping level of $5\times10^{19}\text{cm}^{-3}$ [8, 10]. The values used for simulation are 2 mΩ cm, 122 Wm⁻¹K⁻¹, and –400 µVK⁻¹ respectively for the n-type thermoelements and 5 mΩ cm, 125 Wm⁻¹K⁻¹, and 375 µVK⁻¹ respectively for the p-type thermoelements. These values assume uniform doping of the thermoelements. Due to the small number of long thermoelements, any metal-semiconductor contact resistances is negligible.

As the membrane size increases from a minimum size to support only one thermocouple per quadrant of the device, the number of thermocouples increases and the length of the thermoelements decrease. Accordingly, the voltage increases, the electrical and thermal resistances decrease, and the power delivered to a matched load increases by the relation

$$P_{out} = \left(\frac{4\alpha^2 t_{dev}}{\rho}\right)\left(\frac{W_{leg}}{W_{leg} + W_{il}}\right)\left(\frac{1}{m_{rat} - \frac{10}{9}}\right)\Delta T^2 \qquad (4)$$

where $t_{dev}$ is the thickness of the device layer, $m_{rat} = L_{mod}/L_{mem}$ is the constant describing the module

($L_{mod}$) to membrane length ratio, and $\Delta T$ is the thermal gradient across the thermoelements. This expression assumes a module to rim ($L_{rim}$) length ratio of $L_{mod}/L_{rim} = 20$.
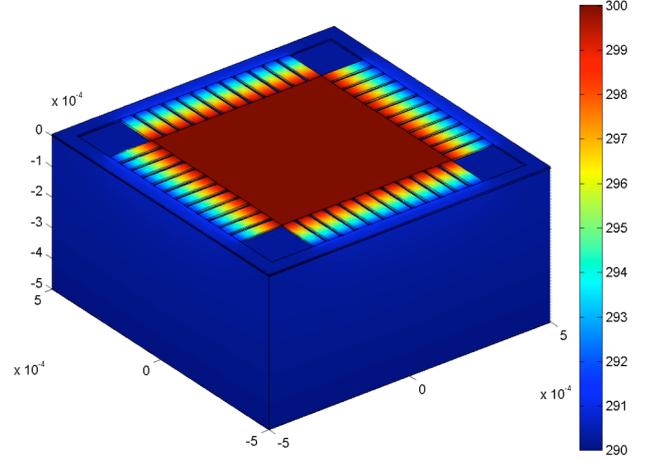


Figure 2: Plot of thermal performance of 24 thermocouple, 1x1mm² SOI-µTEG with the membrane temperature fixed to 300 K and the substrate temperature fixed to 290 K. Each thermoelement is 15 µm wide.
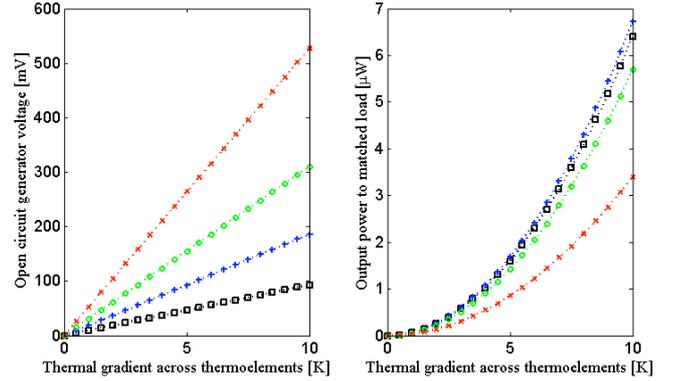


Figure 3: Open circuit voltage and output power to a matched load shown for several leg widths of the 1x1mm² device. Legend for leg widths: black (□), 80 µm; blue (+), 40 µm; green (), 20 µm; red (x), 7 µm.

We first simulated the devices with an enforced 10 K gradient from 300 K at the membrane surface to 290 K at the substrate surface. Figures 2 and 3 show the thermal and electrical characteristics for a device with the module length of 1 mm, membrane length of 600 µm, and thermoelements of length 150 µm a range of widths.

To determine the device performance under more practical conditions for energy harvesting, we also simulated the temperature gradient that results from convective airflow across the substrate. In this case while the membrane temperature is kept constant at 300 K, a rough convective heat transfer coefficient was found from [11] and used to model a convective air flow of 2 ms⁻¹ laterally across the substrate. Table 1 shows performance parameters of the spectrum of devices simulated.

Table 1: Values for structural, electrical, and thermal properties of SOI-µTEG. Length is module length, width is thermoelement width, mem is membrane length, voltage is open circuit voltage with a 10 K gradient across the thermoelements, power is for load matched to generator resistance with a 10 K gradient across the thermoelements, $\Delta T_{10K}$ is the thermal gradient across the thermoelements with a 10K gradient across the device, and $\Delta T_{conv}$ is the thermal gradient across the thermoelements for the previously described convective situation.

| Length [mm] | Width [µm] | Mem [mm] | Voltage @10K [mV] | Power @10K [µW] | $\Delta T_{10K}$ | $\Delta T_{conv}$ |
|---|---|---|---|---|---|---|
| 0.5 | 20 | 0.4 | 250 | 26 | 5.0 | 0.20 |
| 0.5 | 20 | 0.3 | 190 | 6.7 | 7.5 | 0.67 |
| 0.5 | 5 | 0.4 | 620 | 17 | 6.5 | 0.35 |
| 1.0 | 40 | 0.8 | 250 | 26 | 6.5 | 0.26 |
| 1.0 | 7 | 0.6 | 530 | 3.4 | 9.4 | 2.0 |
| 1.0 | 5 | 0.8 | 810 | 11 | 8.3 | 0.66 |
| 2.0 | 80 | 1.6 | 250 | 26 | 8.7 | 0.56 |
| 2.0 | 15 | 1.2 | 530 | 3.6 | 9.6 | 2.7 |
| 2.0 | 14 | 1.6 | 710 | 14 | 8.7 | 0.77 |

## Device Fabrication

We have tailored the design of the generator to bulk semiconductor processes that are available to our group for prototyping. The order of the process flow for fabricating the SOI-µTEG is doping, metallization, reactive ion etching (RIE), and an oxide etch. The first step of the process is to alternately dope the n-type and p-type thermoelements. Diffusion is preferred to ion implantation due to its deeper depth profiles, despite its nonuniform doping concentration. Following the diffusion doping, the intra- and inter-thermoelement contacts must be established through metallization. Chromium interconnect is preferred to aluminum for this device as aluminum has been shown to have similar etch rates to $SiO_2$ when exposed to oxide etchants[12]. The next step is to perforate the membrane and remove the undoped silicon from the rim to the membrane through an RIE etch. The membrane must be perforated to allow the final step, an oxide etch with buffered hydrofluoric acid, to fully release it from the oxide. The distance between adjacent membrane perforation holes must be small enough to allow the isotropic etchant to fully release the membrane. The thermoelements are thin enough to be fully undercut by the isotropic etch.

## Conclusions

To increase the thermal resistance of the heat sink, the wafer handle may be etched to maximize its surface area. We are also considering keeping a small number of residual oxide pillars on the membrane structure to avoid stiction. The parasitic heat flow and post-processing structural isolation of substrate to membrane must be balanced through experimentation. Multiple optimized generators cofabricated on a die may be connected in series to boost the voltage performance. Thermal coupling of the membrane to a heat source is another important consideration in practical applications. Mounting the device on an insulating PCB and mating the membrane with conducting vias that terminate at a large metal plate would provide optimal heat flow from the source.

## References

1. Kiely, J.H., et al., "The design and fabrication of a miniature thermoelectric generator using MOS processing techniques," Meas. Sci. Technol., Vol. 5, No. 2, Feb 1994, pp. 182-189.
2. Glosch, H., et al., "A thermoelectric converter for energy supply," Sensors and Actuators, Vol. 74, Apr 1999, pp. 246-250.
3. Fleurial, J.-P., et al., "Thick-Film Thermoelectric Microdevices," Proc 18th Int. Conf. on Thermoelectrics, Baltimore, MD, Aug/Sept 1999, pp.294-300.
4. Bottner, H., et al., "New thermoelectric components using microsystem technologies," IEEE J. Microelectromech. Syst., Vol. 13, Iss. 3, Jun 2004, pp. 414-420.
5. Strasser, M., et al., "Miniaturized thermoelectric generators based on poly-Si and poly-SiGe surface micromaching," Sensors and Actuators A, Vol. 97-98, Apr 2002, pp. 535-542.
6. Strasser, M., et al., "Micromachined CMOS thermoelectric generators as on-chip power supply," Sensors and Actuators A, Vol. 114, Iss. 2-3, Sept 2004, pp. 362-370.
7. Van Herwaarden, A.W., "The Seebeck Effect in Silicon ICs", Sensors and Actuators, Vol. 6, No. 4 (1984), pp.245-254.
8. Yamashita, O., Sadatomi, N., "Dependence of Seebeck Coefficient on Carrier Concentration in Heavily B- and P-Doped $Si_{1-x}Ge_x (x \le 0.05)$ System," Jpn. J. Appl. Phys., Vol. 38, No. 11, Nov. 1999, pp. 6394-6400.
9. Jacquot, A., et al., "Modeling of on-membrane thermoelectric power supplies," Sensors and Actuators A, Vol. 116, No. 3, Oct 2004, pp 501-508.
10. Burzo, M.G., et al., "Non-contact thermal conductivity measurements of p-doped and n-doped gold covered natural and isotopically-pure silicon and their oxides," Proc 5th Int. Conf. on Thermal and Mechanical Simulation and Experiments in Microelectronics and Microsystems, 2004, pp. 269-276.
11. Incropera, F.P., DeWitt, D.P., Introduction to Heat Transfer, Wiley & Sons (New York, 2002), pp. 381-388.
12. Williams, K.R., et al., "Etch Rates for Micromachining Processing-Part II," IEEE J. Microelectromech. Syst., Vol. 12, No. 6, Dec 2003.