

A 1.56GHz Wide-Tuning All Digital FBAR-Based PLL in 0.13 μm CMOS

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Abstract—This paper presents the design rationale and measured results of a low power, low jitter, PVT-stable FBAR-based RF synthesizer implemented in 0.13 μm CMOS. A digitally controlled FBAR oscillator, tuned with a switched-capacitor array, provides 5800ppm of frequency tuning, sufficient to cover a wide range of manufacturing and temperature variations of an FBAR. An all-digital phase-locked loop (ADPLL) is used to stabilize the FBAR DCO. In the ADPLL architecture, we introduce a two-stage time-to-digital converter (TDC) to detect phase differences between reference and divider clocks. The solution offers a fine TDC resolution without large and power-hungry TDC circuitry typically used to address in-band phase noise requirements. With the tuning range, the power consumption of 2.8 mW, and an integrated RMS jitter of 0.38ps from 10kHz to 20MHz, the FBAR ADPLL provides a PVT-stable, high quality RF frequency reference for a range of low power, high data rate applications.

I. INTRODUCTION

High performance ADCs and high speed RF and wireline transceivers require low jitter, low phase noise RF frequency references for high data rate applications. However, RF frequency synthesizers have reached a bottleneck in performance improvement because of the limited quality factor (Q) in the inductors provided by standard IC processes. Voltage-controlled oscillators (VCOs) using on-chip LC tanks consume a significant amount of power in order to meet stringent phase noise and jitter specifications.

In the past decade, thin film bulk acoustic wave resonators (FBARs) have emerged as a critical building block for miniaturized mobile phone transceivers. The need for high quality RF duplexers and filters has driven the FBAR manufacturing process to maturity [1] [2]. FBAR-based oscillators and frequency synthesizers have demonstrated excellent phase noise performance at extremely low power [3] [4] [5]. FBAR oscillators typically exhibit poor tuning range (< 1000ppm). In this work, we use a high tuning range FBAR DCO in conjunction with an ADPLL to simultaneously realize low power, low noise, and an acceptable tuning range.

Uncompensated FBAR resonators are sensitive to temperature variation with a temperature coefficient (TC) of about -25ppm/ $^{\circ}\text{C}$ [6]. This temperature sensitivity requires an even broader tuning range for an FBAR-based frequency reference than what is needed to cover manufacturing tolerance, which generally falls around 1000ppm. An FBAR-based VCO has to provide an additional 4500ppm in frequency tuning in order to work over a temperature range from -125 to 55 $^{\circ}\text{C}$.

Various efforts have been proposed to stabilize FBAR-based reference frequencies. For instance, physical compensation,

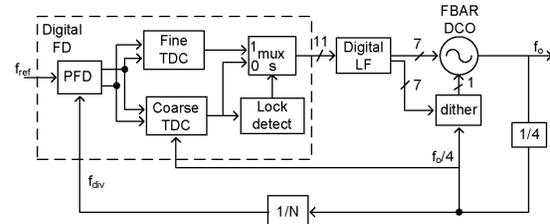


Fig. 1. The proposed ADPLL architecture.

wherein a layer of positive TC material is added to the FBAR stack to cancel the TC of the resonator in the first order, can reduce TC to about 1ppm/ $^{\circ}\text{C}$ [6]. Further frequency stability has been demonstrated through electronic compensation [7], which uses an on-chip temperature sensor to correct frequency changes induced by temperature variation.

This paper presents a technique to implement a wide tuning FBAR oscillator and an all digital PLL (ADPLL) to realize a PVT-stable RF frequency reference with low jitter and low power performance. The FBAR-based ADPLL architecture is shown in Fig.1. Our wide tuning digitally-controlled FBAR oscillator (FBAR DCO) and ADPLL design are described in Sections II and III respectively. The prototyped results based on a 0.13 μm CMOS process are presented in Section IV, along with measured performance figures.

II. THE DIGITALLY-CONTROLLED FBAR OSCILLATOR

A simplified FBAR resonator stack comprises three layers fabricated in a planar process as shown in Fig. 2(a). When electrical energy is applied across the outer electrodes, the piezoelectric inner layer converts the energy into acoustic waves (and vice versa). The mechanical resonator structure is typically around 100 μm x 100 μm , depending on the desired device impedance. FBARs have high quality factors ($Q > 1000$), high power handling capability ($> 1\text{W}$), and the potential to be integrated onto the same silicon substrate as the core CMOS circuitry. The high Q makes it possible to implement low insertion-loss duplexers and filters, and extremely low power, low phase noise VCOs. An FBAR resonator presents a series resonance f_s and a parallel resonance f_p (Fig. 2(b)). The distance between the two resonances is determined by process parameters, which can be quantified by the electro-acoustic coupling coefficient K_t^2 : $K_t^2 = \frac{\pi f_s}{2 f_p \tan[\frac{\pi f_s}{2 f_p}]}$, typically between 3 to 7%. This small value presents a challenge to VCO design, as the distance

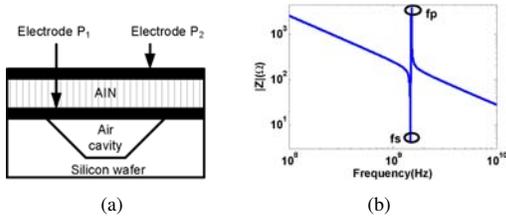


Fig. 2. (a) The FBAR cross-section. (b) The FBAR tank impedance.

between f_p and f_s defines the maximum tuning range using capacitive loading.

We utilize the parallel resonance of the FBAR to design the DCO and implement frequency tuning using a shunt variable capacitor C_L across the FBAR tank. Fig. 3 shows the relation of R_p (the tank impedance at the parallel resonance) and f_p versus C_L for a typical FBAR resonator. As the load capacitor

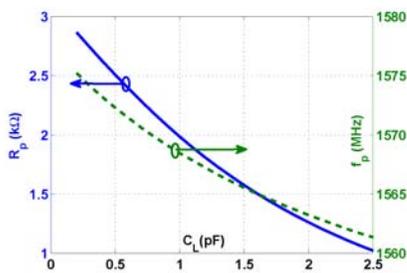


Fig. 3. R_p and f_p as a function of C_L .

C_L increases, the tank impedance R_p drops rapidly and the resonant frequency f_p reduces slowly. Additionally, the FBAR is highly sensitive to capacitive loading. For maximum tuning range, C_L must be minimized.

An efficient tuning device is needed to achieve a wide tuning range DCO. The analog CMOS varactor available in a typical CMOS process has a large parasitic capacitance coupled to the substrate, thus severely limiting the achievable tuning range of an FBAR oscillator [5]. We propose to employ a digitally switched capacitor array to tune an FBAR-based oscillator.

The MIM capacitors available in most CMOS processes are fabricated in the top thick metal layers and have a very small parasitic capacitance ($\sim 1\%$ in our $0.13\mu\text{m}$ CMOS), allowing maximum utilization of the tuning range provided by an FBAR.

Moreover, an FBAR oscillator has a tuning range much smaller ($100\times$) than that of an LC oscillator, allowing us to use a switched array of MIM capacitors, which have a relatively large unit capacitance, without increasing the frequency quantization error.

Fig. 4 shows the architecture of our FBAR DCO implemented with a Pierce oscillator topology with both feedback capacitors C_1 and C_2 used for tuning. C_1 and C_2 have approximately equal tuning sensitivity. The capacitor array is split into two banks, one connected to the drain and the other to the gate of transistor M_n . In order to achieve good linearity in tuning characteristics, the DCO control word is thermometer-coded and the unit capacitors are switched on or off sequentially in

physical order to minimize the impact of process variation [8]. To further increase the frequency resolution and linearity, we alternately index the unit capacitors to the gate and the drain of M_n , effectively adding another bit of resolution.

Our FBAR DCO is loaded with a total of 128 unit capacitors, each of approximately 50fF , providing a 7-bit coarse control to frequency tuning. Since finite frequency resolution in the digitized tuning of the DCO can increase DCO phase noise, we need a higher frequency resolution to completely suppress the quantization-induced phase noise [9]. This is accomplished by adding 7 lower bits and dithering them with a first-order $\Delta\Sigma$ modulator running at $\frac{1}{4}f_o$, where f_o is the ADPLL's output frequency. See Fig. 4(c).

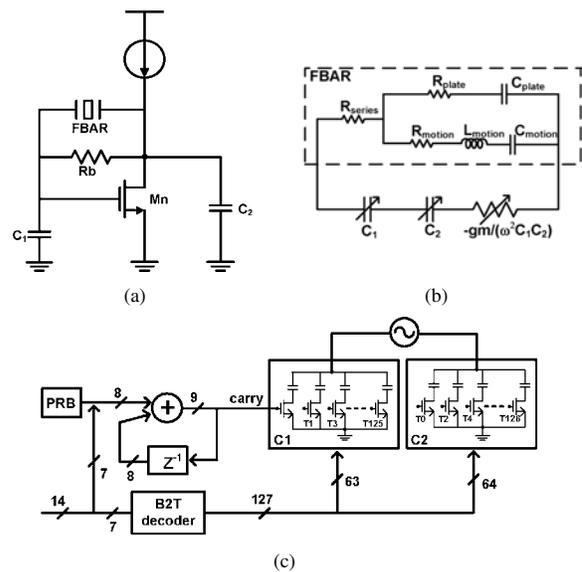


Fig. 4. (a) The FBAR DCO topology. (b) The equivalent small signal model of the FBAR oscillator. (c) Frequency dithering of the FBAR DCO.

III. THE ALL DIGITAL PHASE-LOCKED LOOP

To achieve good long-term frequency accuracy and stability, we lock the wide bandwidth FBAR DCO to a crystal reference through the ADPLL shown in Fig. 1. With the ADPLL, we avoid using an ADC to interface the FBAR DCO to an analog loop filter [10], and large R_s and C_s in a typical low loop bandwidth FBAR PLL [5]. A low-power integer- N divider in true single-phase clock (TSPC) logic, is implemented in the PLL feedback so that the power-hungry phase detector runs at the reference frequency. This, however, requires a long time-to-digital conversion (TDC) to measure the phase difference between the divided frequency and the reference frequency, as the TDC's resolution cannot be compromised. While it is mandatory to keep the TDC at a fine resolution, a long TDC is undesirable since it consumes a large amount of power and area. To address these conflicting requirements, we propose a two-stage TDC scheme in our ADPLL: one coarse and one fine stage.

The digital phase detector is shown in Fig. 5. The coarse TDC detects the phase difference between the reference and

the divider clocks during the phase acquisition state when the phase difference is large. We use a 4-bit counter synchronized with the $\frac{f_o}{4}$ clock to implement the coarse TDC with a resolution of $\Delta T = \frac{4}{f_o}$. When the coarse loop is locked, the contents of the counter (phase difference) is zero and the actual phase difference is pulled within ΔT . The lock detector

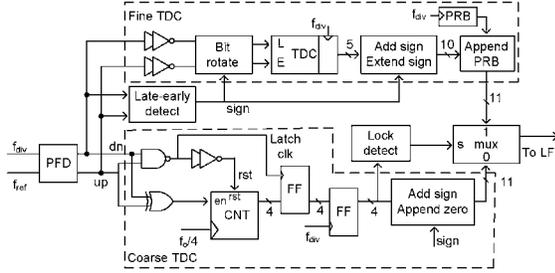


Fig. 5. The digital phase detector.

then generates a ‘1’, and the ADPLL is switched to the fine loop to begin the second locking process. The fine TDC is implemented using a 64-inverter chain. The resolution of the fine TDC, determined by a unit inverter delay of approximately 40ps in our 0.13 μ m CMOS, determines the quantization noise of the TDC and the in-band phase noise of the ADPLL [9]. By matching the phase detector gain for both TDCs, the two loops share the loop filter. The PFD in Figs. 1 and 5, which is a 4-state phase frequency detector commonly used in an analog charge-pump PLL, generates the “up” and “dn” signals. The 4-bit counter is enabled whenever there is a need for “charging up” or “charging down”. The “late-early” detector provides the direction of the “charging current”, which, in our case, is the sign of the phase difference indicated in the counter. Likewise, the inverter chain in the fine TDC detects the absolute phase difference between the reference and the divider clocks with the sign provided by the output of the “late-early” detector. This automated two-step locking process avoids a long, fine-resolution TDC, making it possible to implement the ADPLL in a small area with a low power consumption without sacrificing the phase noise performance or settling time. This ADPLL architecture is directly applicable to LC- or ring-based DCOs.

Feeding to the digital loop filter is the phase difference of the reference frequency and the divided frequency represented by an 11-bit signed binary word. The configurable loop filter consists of a lead and lag IIR and two subsequent single pole IIR filters. The output of the loop filter is a 14-bit unsigned binary that drives the binary input to the FBAR DCO.

IV. EXPERIMENTAL RESULTS

The ADPLL was fabricated in a 0.13 μ m CMOS process, occupying an area of (1.25 \times 0.85)mm² including pads. Both FBAR and CMOS die are directly mounted on a test PCB. Fig. 6 shows a chip micrograph. The DCO draws a current of 0.8mA from a 1.2V supply. The digital loop circuitry consumes 1.5mA from a 1.2V supply.

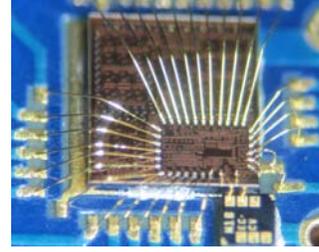


Fig. 6. The chip micrograph.

The measured tuning characteristic of the FBAR DCO is shown in Fig. 7. Fig. 8 shows the measured phase noise of the free running DCO. The FBAR resonator was uncompensated, having a K_t^2 of 5.27% and TC of approximately 25ppm/ $^{\circ}$ C. The DCO achieves a tuning range of 5800ppm. This tuning range allows the FBAR DCO to provide a fixed frequency reference that is immune from normal process and temperature variations. It is also wide enough to provide narrow-band frequency modulations for applications such as serial-ATA (SATA) I/O. The measured ADPLL settling time is about

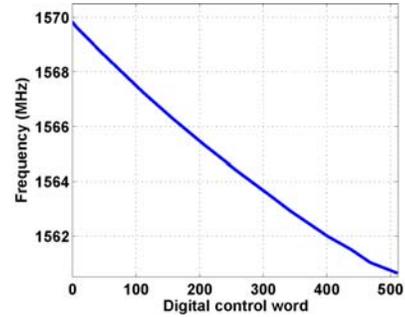


Fig. 7. The measured FBAR DCO tuning curve.

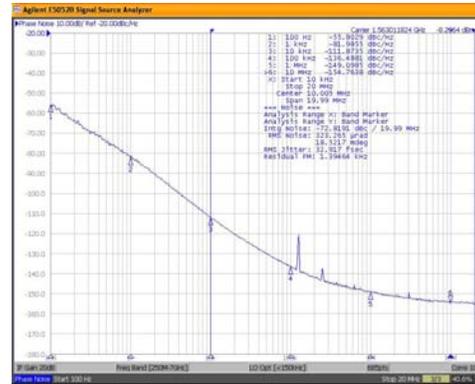


Fig. 8. The measured phase noise of a free running FBAR DCO.

150 μ s (Fig. 9), which is in agreement with the loop bandwidth we set for the PLL. This indicates that the automatically controlled switch between the coarse and fine loops designed in this ADPLL does not introduce glitches or missing cycles during the frequency acquisition and locking process.

Fig.10 shows the ADPLL phase noise when the DCO

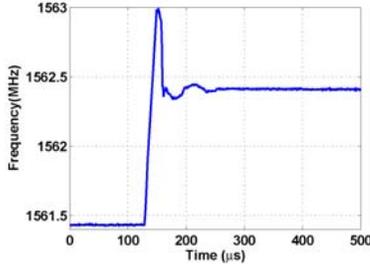


Fig. 9. The measured FBAR ADPLL setting time.

is locked to a 65MHz crystal. The in-band phase noise is around -100dBc/Hz, which is dominated by the TDC quantization noise. The measured phase noise is -101dBc/Hz and -139dBc/Hz at the 10kHz and 1MHz frequency offsets from the 1.56GHz carrier, respectively, both of which are 10dB higher than that of the free running DCO. The elevated phase noise is caused by insufficient frequency dithering of the DCO. The dithering speed was limited to 1/4 of the carrier frequency because our digital adder was not fast enough. With a faster adder in a newer process, the DCO digital quantization can be completely suppressed. The measured integrated RMS jitter from 10k to 20MHz is 385fs. A figure-

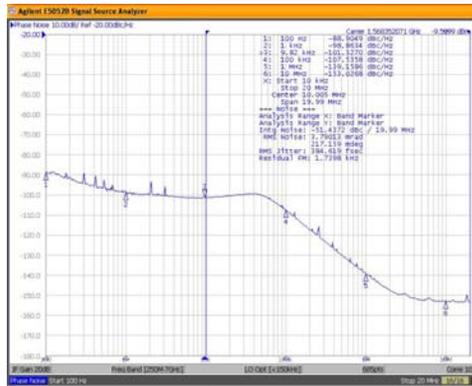


Fig. 10. The measured FBAR ADPLL phase noise performance.

of-merit (FOM) for the frequency reference is assumed to be $FOM = 10 \log_{10} \left(\left(\frac{\delta}{1s} \right)^2 \frac{P}{1mW} \right)$ [11], where δ is the RMS jitter and P is the power consumption of the frequency reference. Fig. 11 shows the FOM of the FBAR ADPLL in comparison with published works.

V. CONCLUSION

We have presented an FBAR-based ADPLL implemented in a 0.13 μ m CMOS process. The FBAR-based DCO is tuned using a digitally switched MIM capacitor array and archives a 5800ppm tuning range, allowing the DCO to cover wide temperature and process variations. It is the widest tuning-range FBAR-based PLL to date. It is nearly completely digital, allowing easy porting to future processes. The ADPLL employs a coarse-fine TDC architecture and provides an RF frequency reference with an RMS jitter of 0.38ps with a power consumption of 2.8mW.

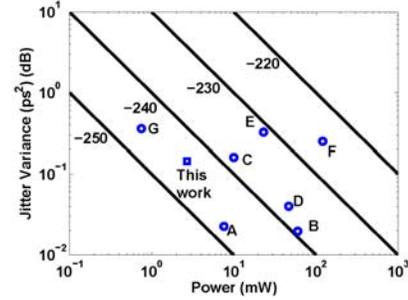


Fig. 11. The FOM of the FBAR ADPLL in comparison with published work. A - [11]; B - [12]; C - [13]; D - [10]; E - [14]; F - [15]; G - [5].

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