Wafer-scale Packaging for FBAR-based Oscillators

Martha Small, Rich Ruby (IEEE Fellow),
Steven Ortiz, Reed Parker
Wireless Semiconductor Division, Avago Technologies
San Jose, California, USA
martha.small@avagotech.com

Fan Zhang, Jianlei Shi, Brian Otis
Department of Electrical Engineering
University of Washington
Seattle, Washington, USA

***Abstract*— Recent advances in temperature-compensation for FBAR (Film Bulk Acoustic Resonators) have brought this technology forward as a serious contender in the oscillator marketplace. As with any mechanical resonator oscillator, a cost-effective hermetic package combined with circuit technology are critical for commercial application. Billions of FBAR duplexers have been fabricated using Avago Technologies' wafer-scale packaging process, whereby a silicon lid wafer is Au-diffusion-bonded to a base FBAR wafer to make a robust, hermetic package. This paper presents a method for integrating circuitry into the lid wafer to form a sub-0.1 mm^3, sub mW, 1.5 GHz temperature-compensated chip-scale oscillator. Circuit integration, testing and performance will be discussed.**

I. INTRODUCTION

For over 20 years, FBAR or SMR-BAW (Solidly-Mounted Resonator – Bulk Acoustic Wave) with its high f•Q product has been proposed as an attractive alternative to conventional approaches for timing applications [1,2]. Like other mm-scale mechanical resonators, FBAR requires a hermetic package in order to maintain frequency stability. The FBAR is also not readily integrated with circuit technologies for the simple reason that the processing that produces the FBAR – high resistivity, high impedance electrodes; high dielectric constant for the piezoelectric material, and highly variable thicknesses depending on the frequency target – does not produce a viable electronic device. Although integrating a Bulk Acoustic resonator or filter on the same substrate as an IC has been demonstrated [3,4,5], there are three problems with this approach: 1) compromises between technologies must be made to eliminate interference between processing steps (e.g. temperature limitations), 2) the economics for integrating the two technologies on the same wafer is unfavorable [6], and 3) none of the previous work addressed the issue of how to create an open-air cavity around the BAW device while simultaneously providing a hermetic and robust package.

Our previous work demonstrated the potential value of an FBAR [7], a wafer scale hermetic package [8], and a modified FBAR demonstrating temperature stability comparable to quartz (referred to as Zero Drift Resonators, or ZDR [9]). We have also demonstrated low noise sub-mW oscillators using FBAR [10]. The work presented here is the culmination of those advancements. We now present a technique for integrating active circuitry into the lid of the wafer-scale hermetic FBAR package while the FBAR resonator, ZDR, or filter resides on the base wafer. Both sides of an opened and "unfolded" module are shown in Figure 1. The 285µm x 330µm active circuit area is clearly visible, as is the location for the FBAR resonator. This strategy is IC technology "agnostic". Besides an area limitation, there are no special circuit design rules required for our technique, and process modification for the lid/IC wafer is minimal compared to a full SOC (system-on-a chip) implementation.

II. PROCESS DESCRIPTION

The wafer fabrication uses existing processes where possible, which has the advantages both of simplicity and of maintaining native device performance. In the Avago microcap process, the FBAR is fabricated on one wafer while a second "lid" wafer contains through-wafer vias, Au pads, sealing structures, and a recessed air cavity above the FBAR.

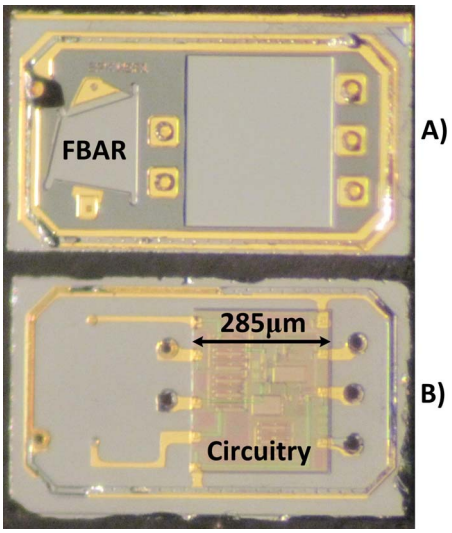

Figure 1. Photograph of disassembled hermetic oscillator package containing A) FBAR die B) lid with integrated active circuitry.

Figure 2 contains a simplified process flow for a standard FBAR/micro-cap part. On the FBAR wafer side, the cavity under the FBAR ("swimming pool") is defined and filled with a sacrificial oxide, the resonators are processed, followed by the patterning of the Au interconnect and sealing material and, finally, the removal of the sacrificial oxide. The Si micro-cap lid is then Au-diffusion bonded to the FBAR wafer and pads patterned on top. The lid wafer is manufactured with standard micromachining processes and through-wafer vias are etched to make external pad connections. Both the FBAR and lid wafers are high-impedance Si to minimize cross-talk and capacitive losses.

Figure 3A contains a schematic flow of the circuit-containing lid wafer. The process flow proceeds as normal with minor modifications for pattern density. Inter-layer dielectric is left in the field until the devices are complete, after which they are removed down to Si. At that point the lid micro-machining can be completed. The cavity etch that leaves a gap above the FBAR removes any remaining epi-Si between contact pads. The final oscillator die with integrated circuitry is shown in Figure 3B. We retained the Au-Au wafer bond that has proven to provide a robust hermetic seal [6]. The circuitry on the lid aligns with a corresponding depression in the FBAR wafer to provide clearance for wafer bonding. Since the depression is patterned along with the depression under the FBAR, no additional masking steps are required. Once the lid is bonded to the FBAR wafer, the lid Au metallization forms the interconnect between the circuitry and the FBAR. Figure 3C contains a SEM cross-section of a bonded die showing the relative position of the FBAR and the lid circuitry (reversed from the schematic). For this demonstration, our circuits used Avago's HP25 silicon bipolar process.

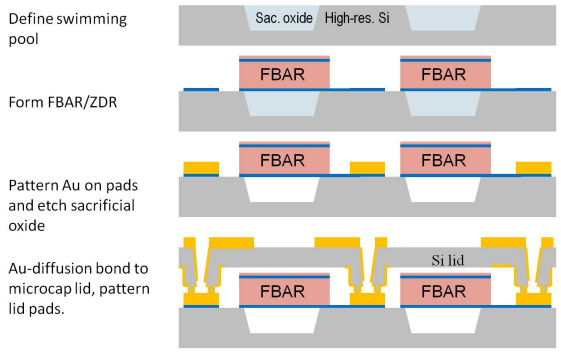

Figure 2. Schematic description of normal FBAR/micro-cap process flow.

III. CIRCUIT IMPLEMENTATION

The concept of integrating active circuitry into the lid has the economic advantage of reusing the lid wafer area for the electronics' pads and from eliminating external connections between the FBAR and the circuit. The size can be further reduced by placing the FBAR directly above the circuitry, which we hope to demonstrate in future iterations. Further economic advantage is gleaned by forcing the circuit size and the resonator (or filter) size to be comparable. The number of external connections is limited by via size; a reasonable via count would be ten or less. In this work, we have six external pads and two internal connections from the lid electronics to the FBAR resonator.

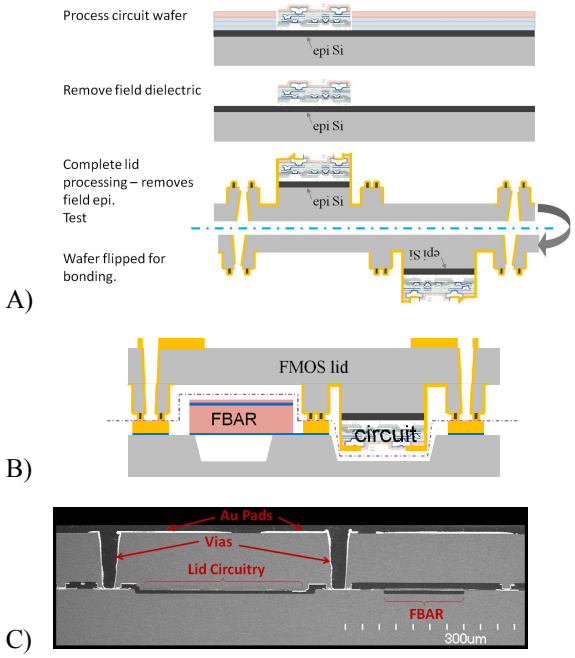

Figure 3. A) Schematic circuit lid flow, B) micro-capped oscillator die, C) cross-section SEM of FBAR/bipolar process showing completed die.

Figure 4A shows the Pierce oscillator and divider that are integrated into the lid. All bias circuitry is integrated and derived internally. The oscillator and bias consume 150µA from a 2V supply. Emitter/Base diode varactors are used for tuning, and a temperature-sensing diode is included for on-die temperature monitoring. The oscillator is AC-coupled to an on-chip divide-by-64 circuit comprising six cascaded stages of divide-by-two bipolar current mode logic (CML). The oscillators operate at 1.5 GHz, yielding a divided clock source of 23.4 MHz. Each divide-by-two circuit includes two cross-coupled D-latches, with the clock input of each latch driven by a level shifter to set the proper DC bias of the input transistors. The maximum operating frequency of the divider-by-two circuit is a function of the D-latch delay and level-shifter delay. The bias currents of the latch and of the level shifter are set accordingly. Because each stage works at half the frequency of the previous one, the bias current of subsequent stages are scaled to reduce power consumption without degrading maximum operating frequency.

A fully-differential Colpitts oscillator was also designed and fabricated in this process. Figure 4B shows the simplified schematic. The Colpitts oscillator has superior cyclostationary noise properties and is thus a good candidate for low jitter reference clocks. However, the Colpitts oscillator requires a higher initial loop gain for oscillator startup. We utilize a gm-boosting technique to reduce power consumption by improving the oscillator startup characteristic. As shown in

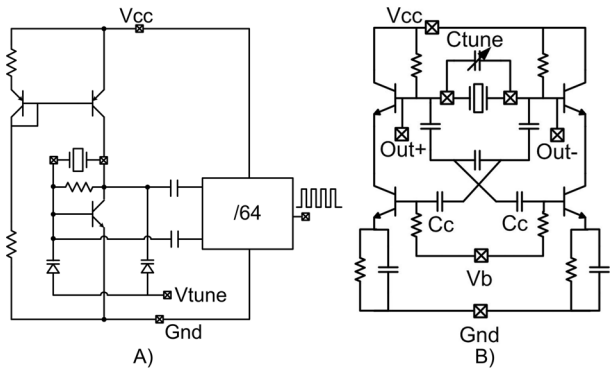

Figure 4. A) Schematic of Pierce oscillator with divider. B) Differential Colpitts oscillator with gm-boosting

Figure 4B, the FBAR resonator is connected between the bases of the top transistor pair. The center point of the FBAR resonator can be viewed as a virtual ground. Differential operation is sustained when the two sides oscillate at opposite phases. By cross-coupling the oscillator output and AC-coupling the signals to the base of the foot transistor pair, the effective loop gain of the oscillator is increased to reduce the bias current requirement. Frequency-dependent emitter degeneration is used to suppress a parasitic mode of oscillation that is not present in typical LC versions of this topology. The differential architecture minimizes common-mode noise introduced power supply and substrate coupling, and thus can further reduce the overall phase noise of the oscillator.

IV. Experimental Results

A. Oscillator Performance

Figure 5 shows the measured transient waveforms from the oscillator at the RF carrier and the divided output. The measured oscillator phase noise at the 1.5 GHz carrier is -118 dBc/Hz @ 100 kHz offset. Although we typically achieve quality factors (Q) of over 2000 for temperature compensated resonators [8], our first devices had a fixable design error limiting the Q of these devices to about 500 to 800. The differential Colpitts oscillator consumes 300µA from a 1.8V supply and provides a phase noise of -124 dBc/Hz @ 100 kHz offset.

These chips integrate temperature compensated FBARs (zero drift resonators, or ZDR) which remove the linear temperature drift around a fixed turn-over temperature (TOT), yielding a residual 2nd order temperature dependence on the order of -15 ppb/˚C^2. The ZDR in these devices have a TOT of approximately -120˚C, which will be moved to 50˚C in subsequent runs. To improve oscillator temperature stability to below 100ppm (over a 100˚C temperature range), a feedback loop measuring temperature is necessary. The on-die temp sensing diode provides a nearly instantaneous read-out of the temperature that closely matches the FBAR temperature. Fig. 6 shows the temperature and frequency as measured by the integrated diode thermometer and a reference sensor placed 10 mm away from the oscillator. A 2W resistive heater on the board was activated for roughly 1 minute to simulate a PA or other heat source. Clearly, the integrated diode will greatly shorten the feedback cycle time and improve temperature compensation accuracy. To test the aging of the wafer-scale packaged resonator, the oscillator frequency shift was measured after 168 hours at 125˚C and again after 336 hours at 125˚C. Less than 1ppm of frequency drift was observed.

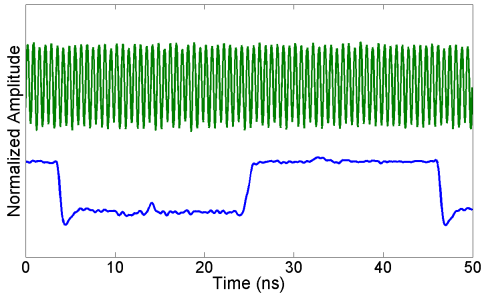

Figure 5. Measured signal at 1.5 GHz RF output (top) and 23.4 MHz divide-by-64 output (bottom)

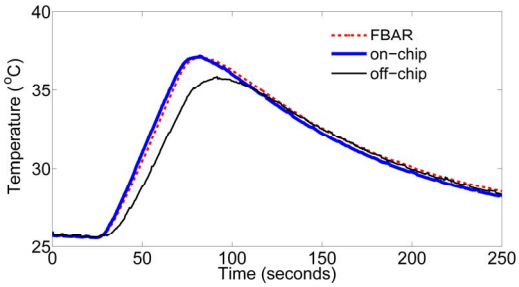

Figure 6. Measured temperature response as measured by the ZDR frequency response, an integrated diode thermometer, and a reference diode placed 10 mm away from the oscillator.

The on-die varactor is used to pull the resonant frequency of the oscillator to compensate for temperature drift as well as any frequency variation due to processing uncertainty. Figure 7 shows the measured pulling range of the oscillator using the integrated varactor (+/- 500 ppm).

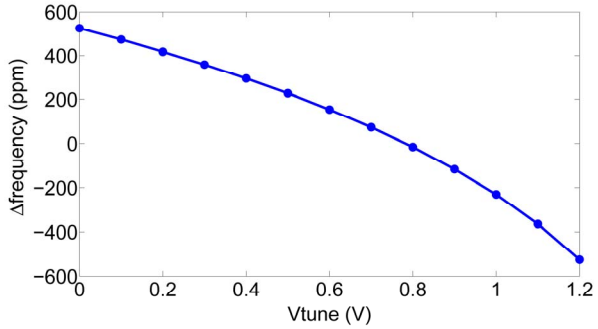

Figure 7. Measured tuning curve of FBAR oscillator.

We used bipolar devices in our first demonstration of this process for three reasons. First, this process has a higher f_T than comparable legacy inexpensive CMOS processes. Secondly, the lower 1/f noise of BJTs provides a significant improvement (6-8dB) in close-in phase noise. Finally, the gm/I_d ratio is 2-3x higher than a MOSFET biased for high f_T.

The properties of this bipolar process thus complement the CMOS circuitry of any accompanying chip.

Different applications of this technology will lead to different optimal partitioning. For example, a high-performance PLL could use the FBAR/bipolar chip as a low noise VCO while the digital functionality were integrated onto a separate CMOS chip. Table 1 is a performance summary of both oscillators implemented in this process. Figure 8 shows the measured phase noise profile of both oscillators.

TABLE I. TABLE 1. DESIGN AND PERFORMANCE SUMMARY

	Pierce	Differential	ISSCC '06 [3]
Integrated FBAR	Yes	Yes	Yes
Hermetic	Yes	Yes	No
Freq (GHz)	1.5	1.5	5.4
Icc (µA)	150	300	1700
Vcc (V)	2.0	1.8	2.7
Tempco (ppm) (0-80˚C)	+/- 200	+/- 200	> +/- 1000*
L(100 Hz) dBc/Hz	-49	-51	-33
L(1 kHz) dBc/Hz	-76	-80	-63
L(10 kHz) dBc/Hz	-98	-104	-93
L(100 kHz) dBc/Hz	-118	-124	-118
*Based on theoretical uncompensated BAW tempco of ~-27ppm/˚C			

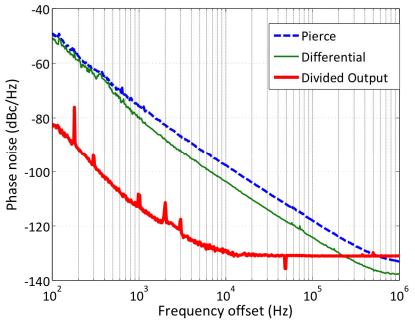

Figure 8. Phase noise of both oscillators measured with an Agilent 5052 signal source analyzer. The 1/f corner for the Pierce is 800 Hz, while the Differential Colpitts is 3 kHz. The phase noise of the ÷64 output is also shown, indicating a 20·log(64) improvement in phase noise. The phase noise floor at 10kHz is the instrument noise floor of the divided output due to a low output signal level. This is not a fundamental limitation.

B. Wafer-level Test

One key benefit of the wafer-scale packaging, as opposed to 2-chip, approach to making FBAR oscillators is the ability to perform wafer-level testing on completed oscillators. Resonator frequency testing with a network analyzer is limited to 5-10 ppm accuracy due to limitations of the measurement and even to parasitic inductance introduced by small variations in probe placement. Oscillator testing reproducibility is <0.2 ppm in initial testing, making it suitable for evaluation of aging effects as well as die screening. Figure 9 shows a map of one of the first wafers made, with the functional ÷64 (23.4 MHz) die shown in green.

V. CONCLUSIONS

We have presented the first circuits implemented in a new single-chip FBAR/Bipolar process. An ultra-low power

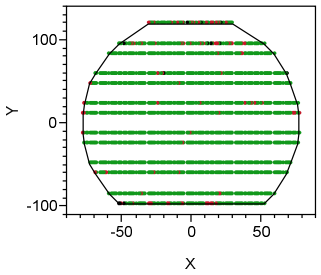

Figure 9. Wafer map showing functional oscillators (in green) from one of the first chip-scale packaged oscillator wafers.

150 µA Pierce oscillator was realized, which achieves a phase noise of -118 dBc/Hz at 100kHz offset. A low noise differential Colpitts oscillator was also implemented, achieving a phase noise of -124 dBc/Hz at 100kHz. The single-chip hermetic package contains all necessary components for a miniaturized frequency reference, including oscillator, high Q resonator, dividers, temperature sensing diode, and frequency tuning varactor.

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