2.8 A 9.2μA Gen 2 Compatible UHF RFID Sensing Tag with -12dBm Sensitivity and 1.25μV$_{rms}$ Input-Referred Noise Floor

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Passive RFID technology enables battery-free wearable and implantable sensors with an unlimited lifespan, small size, and sub-gram weight. These properties facilitate advanced biomedical research (such as untethered monitoring of freely-behaving insects and small animals) and unobtrusive human health monitoring. Passive sensor tags reported to date have employed simple ring oscillator temperature sensors with no protocol or addressability [1,2]. However, realistic applications demand accurate processing of μV-level biosignals and compatibility with industry standard RFID protocols.

We present a fully-passive 900MHz RFID tag IC with addressability, full EPC Class 1 Generation 2 (Gen 2) protocol compatibility, a 1.25μVrms integrated noise chopper-stabilized micropower sensor interface amplifier, and an 8b ADC. The communication range is 3m with an off-the-shelf RFID reader, enabling previously impossible recording scenarios like in-flight recording from small insects. A significant improvement in performance beyond the state-of-the-art was achieved by utilizing a novel self-calibrating on-chip frequency reference, subthreshold digital logic, a low-noise chopper amplifier/ADC, and a unique chip ID generator.

The system architecture is shown in Fig. 2.8.1. Sensor input signals (e.g. EEG, EMG, thermocouple) are first amplified with the on-chip instrumentation amplifier. An 8b SAR ADC digitizes the sensor data. A unique tag ID (UID) is generated by leveraging process variation in the startup configuration of an SRAM, eliminating the need for non-volatile memory [3]. Random numbers (RN) are required in the Gen 2 protocol for random backoff and tag singulation. These are generated by sampling the (unpredictable) clock phase at the downlink baseband edges and passing it through an LFSR. The on-chip controller logic encodes the RN, UID and ADC data into a Gen 2-compatible packet (Fig. 2.8.2) in response to reader commands (Query/ReqRN, Ack, and Read, respectively).

Many tags use a 1.5MHz clock, which requires the tag oscillator PVT stability to meet Gen 2 timing specifications (±15% for 640kHz uplink) as the integer divider residual exceeds the allotted tolerance. Resistor trimming [4], bias current tuning [5], phase locking, and quartz references have been proposed to compensate for PVT variation but are prohibitive due to cost, power and size constraints. We propose a 3MHz temperature-stabilized ring oscillator, shown in Fig. 2.8.3, which lowers the divider residual such that PVT compensation can be performed by the integer divider. The oscillator consumes 260nA from the 0.7V digital supply. We take three approaches to improve stability. First, the divider residual is centered at zero, which reduces the peak residual by a factor of 2. Second, large device size and careful layout limit process variation to 13% (measured). Third, a novel temperature compensation shown in Fig. 2.8.3 tunes the oscillator bias current by measuring and compensating the V_t temperature coefficient. As temperature decreases, f_{osc} decreases. The negative $\Delta V_{gs1}/\Delta T$ coefficient increases the current through $R_{bias,}$ providing the oscillator increased current to compensate for the temperature variation. Careful design of the transistor inversion coefficient and value of $R_{bias,}$ results in a first-order temperature coefficient cancellation.

The RF rectifier employs a 6-stage charge pump topology using zero-V_t devices. An off-chip L-match network transforms the impedance to 50Ω; alternately, this matching network can be easily absorbed into the antenna as in commercial designs. The chip contains a 1.2V bandgap reference and three sub-microwatt regulators: 1.8V (off-chip application-specific components such as micropower opamps), 1.2V (chopper, ADC, UID), and 0.7V (oscillator and digital core). The bandgap reference and the regulators draw 220nA and 300nA, respectively.

Our multi-purpose sensing tag was designed for a variety of sensor interfaces, including biosignal detection, thermocouple readout, and gas detection. These applications demand an extremely low noise floor (<2μVrms input referred) and a relatively low bandwidth (<1kHz). We use a chopper-stabilized topology to suppress 1/f noise and offsets that plague submicron CMOS processes. As shown in Fig. 2.8.4, a fully-differential architecture ensures sufficient linearity, supply rejection, and signal swing under low supply voltages. Dual chopper feedback paths separately set the mid-band gain of the amplifier through C_{FB} and provide input DC bias through high-resistance (>10GΩ) MOS-bipolar pseudo-resistors, thus avoiding additional input-biasing circuitry. The 15pF input capacitance (C_{in}) provides a high (1MΩ at 10kHz) input impedance and prevents loading the electrodes in biomedical applications. The ratio of C_{in} and C_{fb} establishes a 40dB mid-band gain. A programmable 2nd-order G_m-C filter was used to eliminate chopper ripple at the amplifier output.

The chip was fabricated in 0.13μm CMOS with an active area of 2.0mm^2. A performance summary is given in Fig. 2.8.6. The tag was powered and read from an Impinj Speedway reader and 6dBi patch antenna. The RF sensitivity is -12dBm, and the overall tag current consumption is 9.2μA. This is the lowest power biosignal compatible sensor tag presented to date. The digital core consumes 6μA from the 0.7V supply at a 3MHz clock frequency and a 400Hz tag read rate. Oscillator frequency variation is less than 6% from 0 to 95°C, including the on-chip bias and supply voltage generation. This enables the post divider clock to operate over a compensated range of 640kHz ±15% to 40kHz ±4% including PVT variations as per the Gen 2 specification. The chopper amplifier consumes 1.2μA from the 1.2V supply. As shown in Fig. 2.8.4, the gain is 38.5dB with and without the internally-generated 10kHz chopper clock. A high-pass corner at 0.2Hz exists when the chopper clock is off; while the gain is flat to DC with chopping enabled. The input-referred noise from 0.05 to 100Hz is 1.25μVrms and 4.26μVrms with chopping on and off, respectively.

Figure 2.8.7 shows the PCB, which measures less than 1cm^2 and weighs 0.25g. Additional gain can be configured using on-board 1.8V micropower opamps. The system was mounted on a Manduca Sexta (Hawkmoth) and used to record the in-flight core body temperature using a 36AWG Type-T (copper–constantan) thermocouple. This moth species generates a substantial temperature increase from ambient before flight. This research is traditionally performed with a wired thermocouple implanted in a tethered moth. Our wireless, battery-free experimental setup and *in vivo* data are shown in Fig. 2.8.5. The thermocouple was implanted in the Dorsal Longitudinal wing muscle, and real-time temperature during moth warm-up (100 samples/second) is plotted versus time. Including the antenna and thermocouple, the entire system weighs 0.35g. The power of our moth-worn system is two orders of magnitude lower than an active radio-based tag [6]. This work enables the first long-term in-flight recording of an insect by removing both the wires and batteries from the recording equipment.

Acknowledgements:
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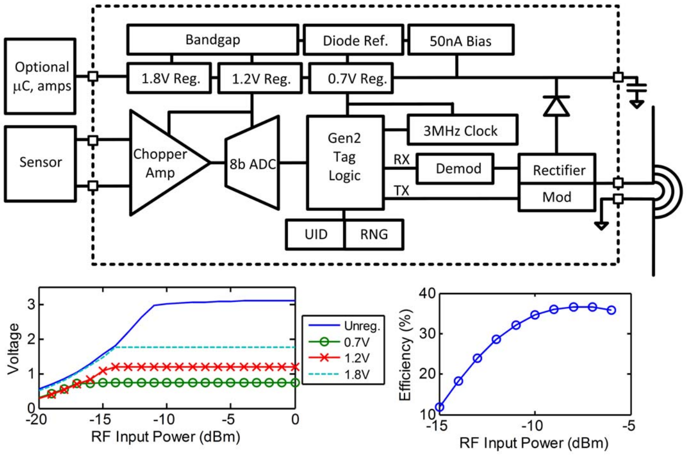


Figure 2.8.1: System architecture and performance.

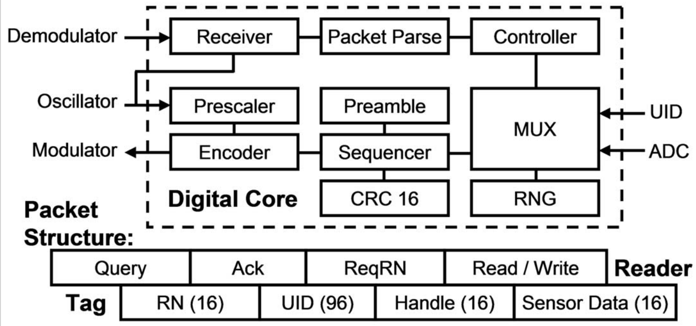


Figure 2.8.2: Digital core and packet structure.

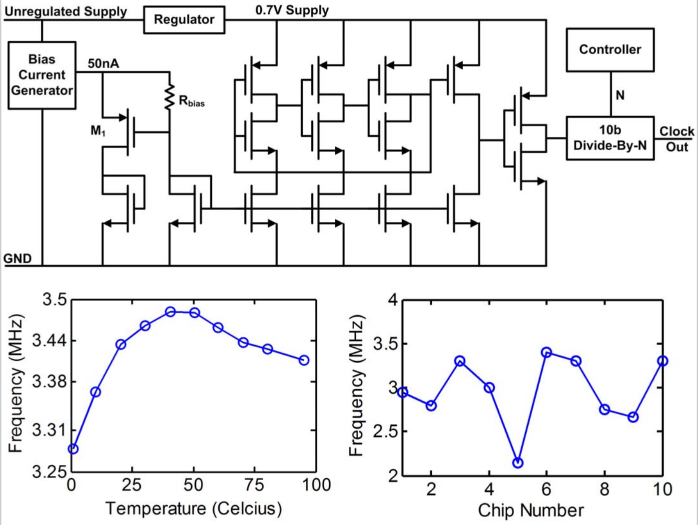


Figure 2.8.3: Oscillator schematic and performance.

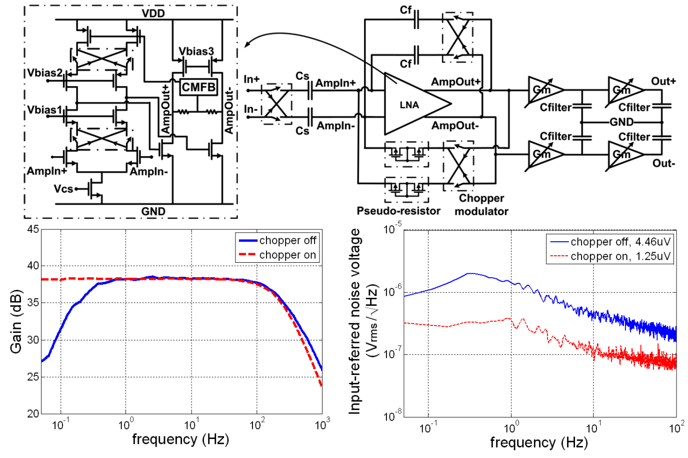
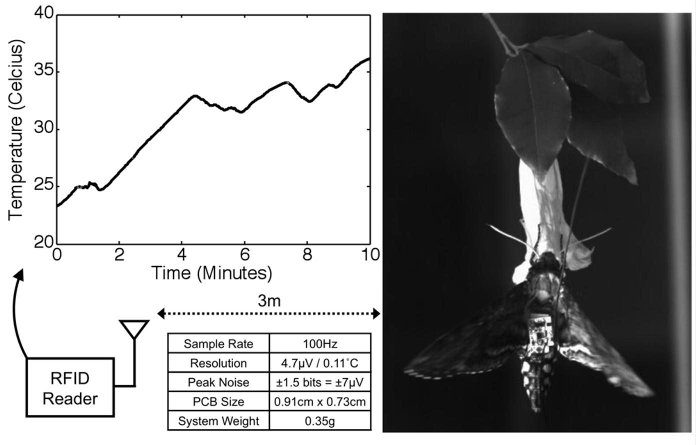


Figure 2.8.4: LNA schematic, gain and noise versus frequency.



Sample Rate	100Hz
Resolution	4.7µV / 0.11˚C
Peak Noise	±1.5 bits = ±7µV
PCB Size	0.91cm x 0.73cm
System Weight	0.35g

Figure 2.8.5: In vivo data and deployment photograph.

Chopper:

	This work	[7]
Power (µW)	1.44	1.8-3.3
Supply (V)	1.2	1.8-3.3
Gain (dB)	38.5	41/50.5
Bandwidth (Hz)	230	180
Input-referred noise (μV_{rms})	1.25	0.95
NEF	5.04	4.03 /4.76
CMRR (dB)	>70	>80
THD (Vin=5mV)	<0.05%	<0.1%
Topology	Fully-Differential	Single-Ended

System:

Current Consumption	9.2µA
Unregulated Voltage	1.8V – 3.6V
RF Sensitivity	-12dBm
Peak Efficiency	37%
IC Area	2.0mm²
Components:	
Analog Core	1.2µA
Reference Oscillator	260nA
Digital Core	6µA
ADC & UID	500nA
Chopper Amp	1.2µA

Figure 2.8.6: Performance metrics and current consumption breakdown.

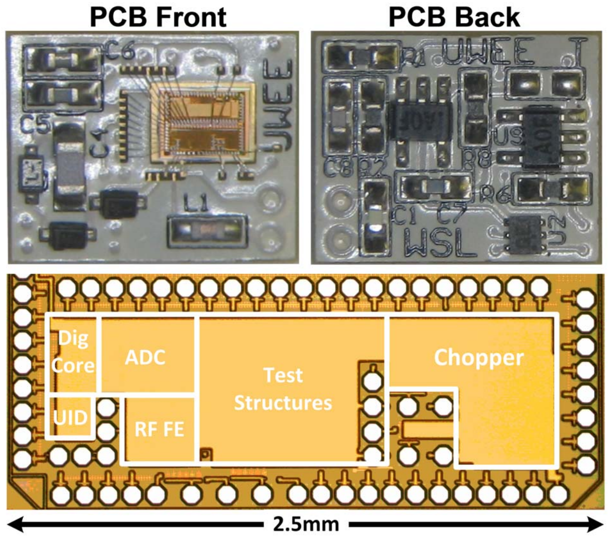


Figure 2.8.7: Chip and PCB micrographs.

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