An Ultra-Low Power MEMS-Based Two-Channel Transceiver for Wireless Sensor Networks

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Abstract

This paper explores the design and implementation of a low-power two-channel transceiver using micromachined resonators. Wireless sensor networks require transceivers that are small, cheap, and power efficient. RF-MEMS resonators are utilized to accommodate these constraints. The prototype 1.9GHz transceiver, designed in 0.13µm CMOS, operates at 1.2V and consumes 3mA in receive mode and transmits 1.6dBm with 17% efficiency. The two 40kb/s channels achieve a sensitivity of –78dBm with a 10µs receiver start-up time.

Keywords: wireless sensor networks, low power transceivers and RF-MEMS

Introduction

A. Design Goals

The transceiver specifications for wireless sensor networks demand extremely low power consumption, very high levels of integration, and a fast turn-on time for both the transmitter and receiver [1]. These requirements ensure that the transceiver and its energy source will be small and cheap, enabling deployment in quantities sufficient to create a truly ambient intelligent environment. Due to the heavily duty-cycled nature of these systems, long transceiver turn-on times dramatically degrade the global efficiency of the system. The level of radio integration must be high, eliminating the possibility of some standard radio components such as quartz crystals.

B. MEMS Components

To address these stringent requirements, a new and emerging technology was investigated: RF-MEMS resonators. Recently, much progress has been made on GHz-range MEMS resonators, typically for use in bandpass filters and duplexers [2][3]. Since these resonators exhibit quality (Q) factors greater than 1000, these devices have the potential to facilitate the design of low power RF transceivers. The presence of an RF frequency reference can eliminate the need for quartz crystals in the system, greatly increasing the level of integration and decreasing the cost. For this implementation, Thin-Film Bulk Acoustic Wave (FBAR) resonators produced by Agilent Technologies [3] were used, which exhibit resonant frequencies at approximately 1.9GHz. This relatively high carrier frequency allows the use of small chip antennas, further increasing system integration [4].

Receiver Design

A. Receiver Architecture

The receiver block diagram is shown in Fig. 1. The two-channel tuned radio frequency (TRF) architecture was chosen to demonstrate the effectiveness of RF-MEMS resonators in low power transceivers.

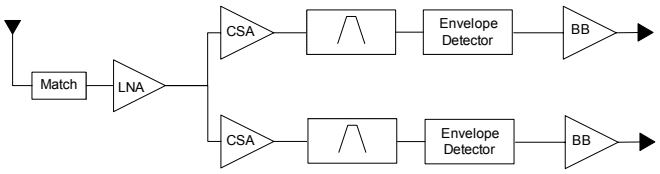

Fig. 1 Receiver Architecture

The antenna feeds a 50Ω impedance presented by the LNA. The LNA drives a tuned load consisting of two channel select amplifiers (CSAs). Although two channels were used in this implementation, this architecture is scalable to larger numbers of channels. Each CSA is tuned by an FBAR resonator, which performs receiver channel selection. The CSAs drive an envelope detector, which acts as a self-mixer to perform signal downconversion. Baseband buffers are included to drive test instrumentation. Since the frequency stabilization is performed entirely by the MEMS resonators, no quartz crystals are used in this receiver architecture. The absence of a phase-locked loop (PLL) ensures a much faster receiver start-up time than a traditional radio.

The two-channel embodiment displays flexibility in terms of modulation schemes: the receiver can detect two unique OOK data streams at two carrier frequencies or it can detect FSK. For dense wireless sensor networks, it is anticipated that two separate OOK channels will be used, with one reserved for beaconing. Changing between these two modulation schemes can be accomplished with no receiver modifications, and can be performed dynamically in either the analog or digital baseband detection circuitry.

B. LNA

The low noise amplifier must achieve high gain and moderate noise figure while simultaneously providing input impedance matching. In order to satisfy these requirements, the architecture shown in Fig. 2 was implemented. The non-quasi static (NQS) gate resistance of the input transistor was transformed via a passive matching network to match the 50Ω source resistance. The NQS gate resistance is inversely proportional to the device transconductance, and is especially pronounced at low current levels [5]. An off-chip matching inductor (L_g) was used for maximum flexibility in the prototyping phase, but it could easily be integrated on-chip.

The parasitic capacitance C_p results from ESD diodes, bond pads, and board and layout traces. For a given bias cur-

rent and fixed C_p, an optimal device size exists that maximizes the f_t. The output tank inductor was implemented on-chip by shunting the two top-level metal layers in order to increase the quality factor. It was characterized using a 3D electromagnetic solver and verified experimentally.

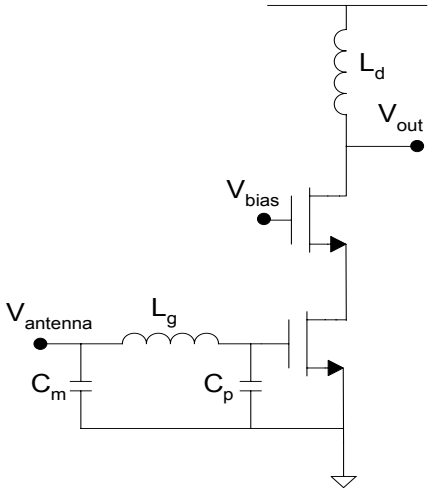

Fig. 2 LNA Schematic

C. Channel Select Amplifier/MEMS Co-design

The channel select amplifier provides high RF gain to overcome the high noise figure of the detector as well as to interface the electrical signal with the acoustic resonator to perform high-Q filtering of the signal. The amplifier must exhibit high RF gain with a low power consumption while limiting the extent to which the resonator is de-tuned. See Fig. 3 for the schematic.

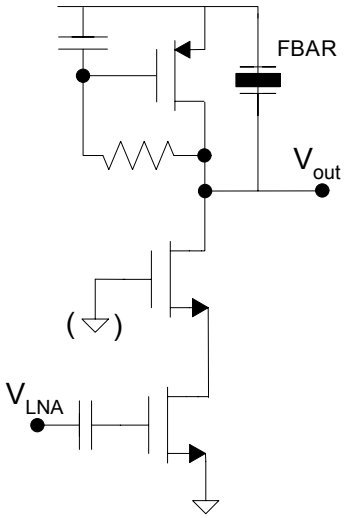

Fig. 3 Channel Select Amplifier Schematic

The amplifier consists of an NMOS cascode transconductance stage and a tuned load. The amplifier input capacitance is absorbed into the LNA load. A cascode transconductor structure is used to increase reverse isolation, ensuring amplifier stability. The tuned load consists of an FBAR resonator to perform channel selection and an inductive PMOS-R-C structure, which stabilizes the low-frequency bias point of the amplifier. The loaded quality factor of the tuned load is approximately 600, yielding an RF bandwidth of 3MHz.

D. Baseband Design

The on-chip baseband circuitry downconverts the OOK or FSK modulated data to DC, performs filtering, and buffers the signal for driving subsequent instrumentation or circuitry. The first baseband block, shown in the Fig. 4, is a non-linear low pass filter, or envelope detector. This circuit, composed of MOSFETs biased in the deep subthreshold regime, performs a self-mixing operation on the RF signal that has been filtered by the channel-select amplifiers.

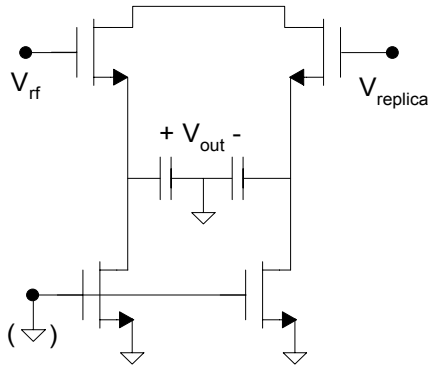

Fig. 4 Envelope Detector Schematic

The low-pass filter has a 300kHz cutoff frequency that attenuates all fundamental tones passing through the receive chain. A replica envelope detector provides a reference DC level, producing a pseudo-differential baseband output. The current consumption of each detector is 200nA.

Each channel in the receive chain also contains a low-power buffer to drive off-chip instrumentation. The buffers are capable of driving a 20pF off-chip load while consuming 50μA. On-chip threshold-referenced bias circuits provide a moderate level of power-supply independence.

Transmitter Design

A. Transmitter Architecture

In a typical sensor network, the transmitter sends out sporadic bursts of short data packets to neighboring sensor nodes (< 10m). For a receiver sensitivity of –60dBm and indoor multi-path fading conditions, the application of the Friis wave propagation equation [6] shows that a transmit power of about 0dBm is required. The transmitter must exhibit fast turn-on time and high efficiency. The transmitter architecture shown in Fig. 5 is well-suited for these requirements.

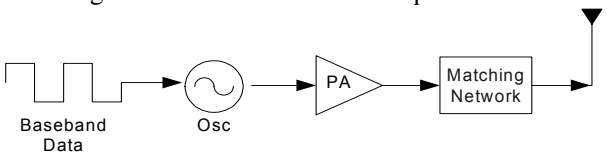

Fig. 5 Direct modulation transmitter architecture

The MEMS-based oscillator is directly modulated by the baseband data and the power amplifier efficiently boosts the RF signal power. Direct modulation eliminates power hungry mixers and PLLs. Multiple channels can be implemented by tuning the oscillation frequency, or by adding oscillators/transmit chains in parallel.

B. Oscillator

In this implementation, carrier generation is accomplished with an oscillator co-designed with an FBAR resonator [7]. This architecture provides a low power 1.9GHz frequency reference without a PLL and quartz crystal reference. In addition, the start-up time is approximately 1µs, enabling the oscillator to be power cycled between transmitted bits, increasing the overall efficiency of the transmitter.

C. Power Amplifier

The schematic of the low-power amplifier is shown in Fig. 6.

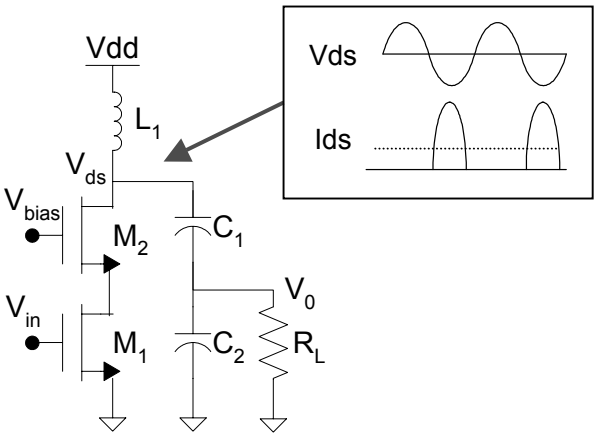

Fig. 6 Schematic of the low-power amplifier

Maximizing the drain efficiency requires the voltage swing V_{ds} to be maximized. For 1.2mW output power with a 1.2V supply and 100mV knee voltage, a 500Ω load resistance at the drain of M2 is required. To achieve this, the 50Ω antenna (R_L) is transformed to the required impedance using C_1 and C_2. Inductor L_1 tunes out the transformed capacitance and the parasitic drain capacitance. Capacitive transformers are preferred over LC matching networks or inductive transformers because on-chip capacitors have much higher Q (>50) than on-chip inductors (Q of 5–10), resulting in less loss. In the current prototype, the required L_1 is 1.2nH and is implemented using an off-chip inductor. However, a short bond wire or an on-chip inductor can be used for a fully integrated solution.

Cascode transistor M2 ensures that the drain voltage does not exceed the low gate breakdown voltage for deep sub-micron CMOS. Cascoding increases the isolation between the input and output and improves the efficiency by boosting the drain resistance of M2.

Implementation

The transceiver was implemented in a standard 0.13µm CMOS process. The complete transceiver system is shown in Fig. 7. The chip area is (4x4)mm^2, which is mostly consumed by passive test structures. The actual transceiver area consumed is approximately 8mm^2. Chip-on-board (COB) wirebonding was used to interface to the chip. As shown in the system photograph, the four FBAR resonators are bonded directly to the chip using standard COB wirebonding. This eliminates board parasitics on these sensitive nodes and reduces the required board area.

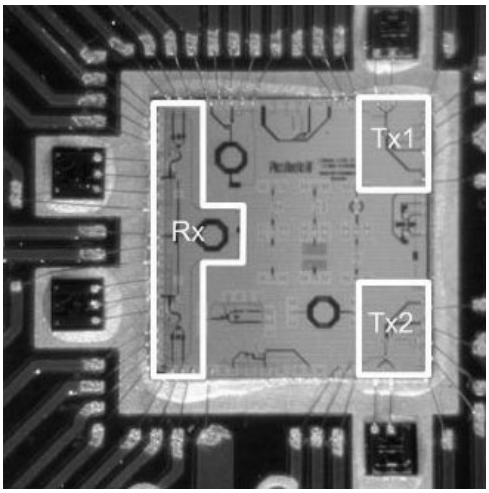

Fig. 7 Transceiver Photograph

Measured Results

The testboard was connected to a single 1.2V supply. The input matching of the LNA showed an S11 of approximately –10dB in the receive frequency band. The measured S21 of a standalone channel select amp is shown in Fig. 8.

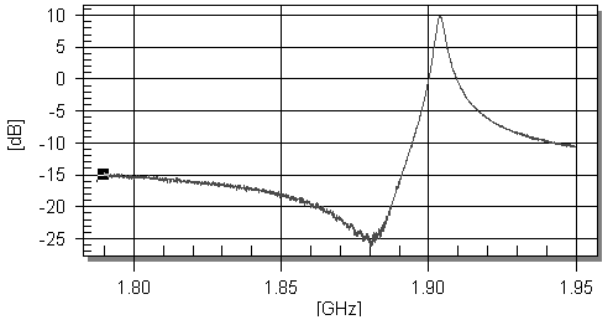

Fig. 8 Measured S21 of Channel Select Amplifier

This corresponds to an in-situ voltage gain of approximately 16dB and a –3dB bandwidth of 3MHz, indicating a loaded quality factor of over 600 for the CMOS/FBAR amplifier. The normalized receiver gain of both channels is shown in Fig. 9.

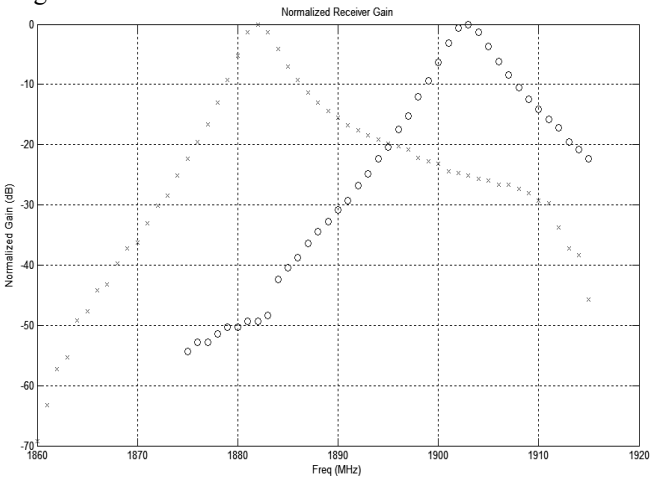

Fig. 9 Normalized Receiver Gain

Both receive channels exhibit a 3MHz bandwidth and close gain matching. Receiver sensitivity for a 12dB SNR was

measured at –78dBm. As mentioned in Section I, the start-up time of the receiver is crucial in a wireless sensor network application. Fig. 10 shows the receiver start-up transient.

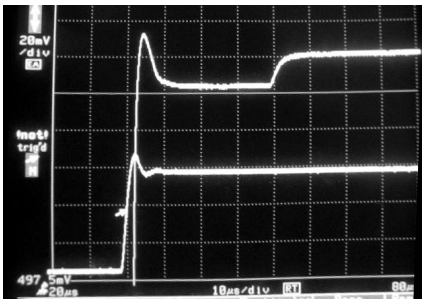

Fig. 10 Receiver Start-Up (10µs/div)

The bottom trace is a 0 to V_{dd} transient. The top trace is the baseband output in the presence of a 20kbps OOK input signal. The measured start-up time is 10µs, minimizing the overhead associated with heavy duty-cycling. The total receiver current consumption was 3mA. The component current breakdown is shown below in Fig. 11.

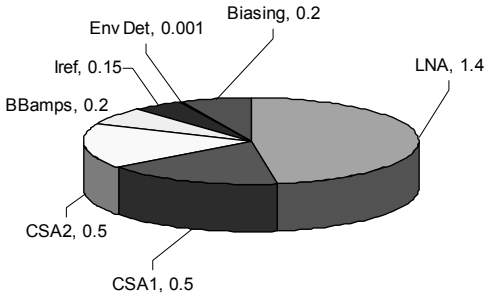

Fig. 11 Receive Current Consumption Breakdown (mA)

Fig. 12 shows the measured transmitter efficiency for both transmit channels for various output power levels. The peak efficiency for the low frequency (LF) and high frequency (HF) channels are 16.5% and 14.7% respectively, and occur at an output power of 1.45mW. Higher efficiency is observed for the LF channel due to better alignment between the oscillator resonant tank and the power amplifier output filter.

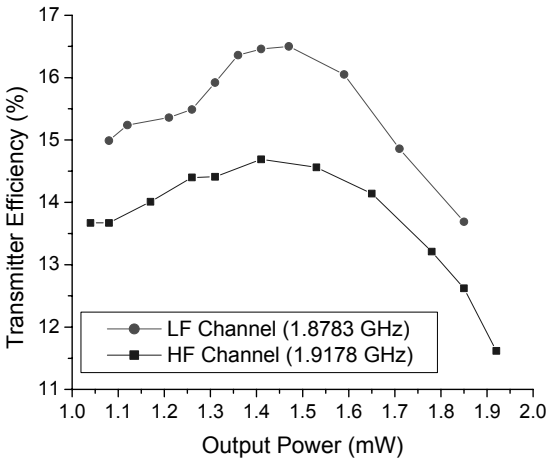

Fig. 12 Transmitter efficiency versus output power

At an output power of 0dBm, the measured HD_2 and HD_3 for the LF channel are –38.4dB and –45.3dB below the carrier, respectively. For the HF channel, the measured HD_2 and HD_3 are –35.0dB and –45.7dB respectively. Table I compares measured performance to existing designs.

TABLE I
Comparison with Existing Transmitter Work

	[8]	[9]	This work
Frequency	2.4 GHz	434 MHz	1.9 GHz
CMOS Process	0.18µm	0.5µm	0.13µm
Supply voltage	1.2V	1V (1.2V)	1.2V
Output Power	1mW	1mW (10mW)	1.4mW
TX efficiency	5.6%	17% (38%)	16.5%

Conclusions

This work has demonstrated the possibility of using RF-MEMS components in the design of a low power transceiver. RF-MEMS/CMOS co-design techniques have enabled a low power receiver with a 10µs turn-on time. For prototyping reasons, two surface-mount (1.2nH and 8nH) inductors were used. Since the quality factor requirements are not stringent, these inductors could easily be integrated on the chip, yielding a transceiver with no external or surface mount components.

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